

Low-power Design of Digital Integrated Circuit Based on UPF Standard

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Abstract. At present, power consumption has become a factor in design of integrated circuit with growing concern in addition to timing and area. Currently, there are many methods to reduce power consumption. In the paper, standard complete technique of Unified Power Format (UPF) based on IEEE1801 standard is used in the design realization and verification process of one chip in order to utilize various design methods of low power consumption more effectively in design implementation flow. The whole process from RTL to GDSII is successfully completed. Chip test is successfully completed. In the paper, the design realization part thereof is discussed in details. How to describe low power consumption intention with UPF and how to use Synopsys tool to realize the whole process are mainly introduced. In the paper, some methods of low power consumption design are firstly introduced, which are commonly used at present, the realization method with power-gating is specially utilized to control statistic power consumption and UPF. Then, the application of UPF in the design is described, and conclusion is given finally.

1. Introduction

IC design is faced with many challenges with process feature dimension reduction and complexity improvement: speed is higher and higher, area is constantly increased, and noise phenomenon is more and more serious, etc. [1]. Wherein, the power dissipation problem is particularly prominent. After the craft enters into node under 130nm, the power consumption density on unit area is sharply increased, which has been up to the limit, which can be supported by encapsulation, heat dissipation and underlying equipment. When the craft continuously reaches below 90 nm, the leakage current is increased exponentially. Leakage current is as big as dynamic current in some 65 nm designs. Static power consumption which can be ignored previously becomes main part of power consumption. Power consumption has become the third dimension element following the traditional two-dimensional elements (speed and area) [2].

In addition, higher and higher requirements are also proposed to low power consumption in current handheld electronic equipment market with rapid development in order to strengthen the competitiveness of own products; Secondly, it is required that IC power consumption should be lower and lower due to cooling and reliability problems. Finally, the concept of green technology environmental protection, environment-friendliness and energy-saving are advocated all over the world [3]. Therefore, it is required that technology with low power consumption must be adopted during IC design, thereby effectively coping with these challenges.

2. Current situation of UPF low power consumption development

2.1 Current commonly-used methods for low power consumption design

Factors affecting power consumption include voltage, leakage current, working frequency, effective capacitance, etc. Dynamic power consumption can be reduced through reducing working voltage, reducing turnover load, reducing circuit turnover rate, etc. Static power consumption can be reduced through reducing working voltage and lowering leakage current [4]. At present, various methods are adopted in the industry to reduce dynamic power consumption and static power consumption of the chip. Traditional low-power technologies include clock-gating, multi-threshold

libraries, etc.; newer technologies include multi-voltage, power gating, power gating with state retention, dynamic voltage and frequency scaling, low-V_{dd} standby, etc. [5].

2.2 Methods to control static electric leakage

2.2.1 Gate-level optimization

In the process of design implementation, automated synthesis and layout wiring tools can comprehensively utilize timing, area and power consumption of all standard units for each path according to the temporal characteristics of the circuit. Standard units in non-critical paths are switched to units with smaller driving ability according to load. Since the output capacitance is reduced, dynamic power consumption can be reduced; meanwhile, since standard cell MOS tube and capacitance are decreased, the static leakage current is also reduced. The purpose of lowering power consumption also can be achieved through optimizing physical locations of logical unit and mobile unit in the circuit, etc..

2.2.2 Multi-threshold libraries

High threshold voltage standard unit is characterized by small leakage current and slow speed. Low threshold voltage standard unit is characterized by faster speed and large leakage current. Therefore, multi-threshold libraries are adopted as target libraries realized in the design. High-threshold voltage standard unit can be utilized as far as possible in the design. Standard unit of low-threshold voltage can be adopted on key path in order to meet timing requirements, thereby reducing leakage current of standard unit maximally, and reducing static power consumption .

2.2.3 Power Gating

When some modules in the chip are not operated, the power supply can be turned off. When they should be operated, the power supply can be connected, and this is Power Gating technique. Leakage current in the Power Gating area can be dropped to zero, thereby greatly reducing the static power consumption of the chip. Currently, there are also many technologies of Power Gating, including shutoff in the chip and shutoff outside the chip. As the name implies, shutoff outside the chip refers that some modules in the chip can be shut off through cutting off the power supply outside the chip. Shutoff inside the chip is further divided into fine-grain and coarse-grain. Fine-grain should be supported by special library, and fine-grain of each standard unit can be realized. Power supply or ground of some modules can be controlled only through some gate control unit in coarse-grain. The pmos is used for controlling power supply, and nmos can be used for controlling ground.

3. Digital integrated circuit low power consumption design realization process based on UPF standard

3.1 Digital integrated circuit low power consumption design principle of Synopsys based on UPF standard

IEEE1801 standard Unified Power Format (UPF) is a low power implementation standard which is truly unified and widely used. Some standard statements are used for describing use low power design intent.

The whole IC design implementation authentication flow can be completed according to description in UPF on low power design intent in the aspects of logic synthesis, physical implementation, simulation verification, equivalence checking and final sign-off process by such a unified UPF file. Low-power intent penetrating through the whole flow is originated from the same file. The risk of low-power design can be greatly reduced by the consistency. In addition, open flow and solutions supported by tools of many manufacturers are provided by UPF on low-consumption design. It is proved that UPF is a standard with strong interoperability by many products of EDA supporting UPF standard.

3.2 Digital integrated circuit low power consumption design flow of Synopsys based on UPF standard

Synopsys Company provides complete UPF-based low power consumption integration, physical implementation and validation process as shown in figure 1. The process begins with logic design of

register transfer level (RTL) description plus a separate UPF file for description of low power design intent. RTL and UPF descriptions are respectively placed in separate files so that they can be maintained and modified separately. In the case, the initial UPF file is marked as UPF.

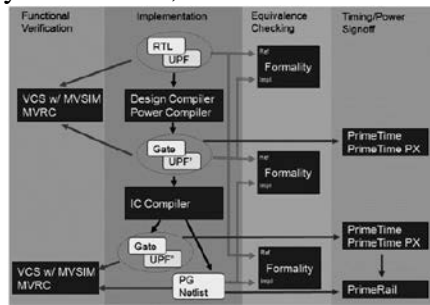


Fig. 1 UPF flow of Synopsys tool

Design Compiler reads in RTL and initial UPF description file. Since they integrate gate-level netlist and produce an updated UPF file, the UPF document output by the Design Compiler is marked as UPF' in typical drawing. UPF' file contains the content of the original UPF file. Power supply and ground connection relationship of some special cells added during integration is also added (such as isolation cells and level shifters). Some special circuit units for low power consumption are inserted according to corresponding description of UPF by tools in gate-level netlist for comprehensively output, such as Level Shifter, Isolation cells, Retention Register, etc.

IC Compiler reads gate-level netlist of integrated output and UPF' description files. They can achieve physical implementation on the basis, including: insertion of layout, wiring and power gating special unit, connection of placement and control signal line, etc. One new gate-level netlist, one netlist including all cell power supplies and ground connection relationships (commonly known as pg netlist) and one updated UPF file marked as UPF'' are output. UPF'' file includes contents of UPF'. Change on low power circuit structure is added at the stage physical implementation, such as addition of connection relationship of Power Switches (commonly known as MTCMOS).

Data produced in the flow can be used for function simulation (utilization of MVSIM and VCS), correctness check of inserted low power unit (utilization of MVRC), formal verification (utilization of Formality), temporal power inspection (utilization of Prime Time - PX) and voltage drop (IR-Drop) verification.

VCS simulator and MVSIM Multi-Voltage simulation tools can be used for function simulation of Multi-Voltage at several stages: RTL level: gate level of low-power related devices is added after integration (such as the Isolation cell); gate level of Power Switches is added after PR. MVRC is used for checking whether the rules of Multi - Voltage design is correctly implemented or not, including power supply connection relations, power supply structure, power supply consistency, etc., and it also can be applied to different steps in the process.

Prime Time reads in gate-level netlist of DC or ICC output and corresponding UPF files. It utilizes information in UPF file to establish a virtual power network model, and voltage value is labeled to each device power supply port. Timing inspection with power supply information is implemented.

Prime Rail is used for analyzing voltage drop and electro-migration based on territory with UPF information. If there is power gating unit in the design, it also can be used for analyzing transient current dynamic distribution of voltage drop about switch-off circuit, thereby assisting in judging whether these power gating units are inserted reasonably or not and whether De-cap unit should be inserted or not.

4. Special cell library for UPF

UPF-based design process is compared with traditional process. UPF-based design process should be supported by some special units in the library. Power supply ground information is added on traditional DB timing library. Special units include Level shifter, Isolation Cell, Power Gating unit (also called MTCMOS), Retention-Register and Always - on unit.

4.1 Level-Shifter and Isolation Cell

Level-shifter has to be used to realize signal level conversion of signals among different voltage domains aiming at multi-voltage design. Level-shifters are divided into two categories according to conversion of signal level from top to bottom and from bottom to top. The structure is respectively shown in Figure 2 and Figure 3.



Fig. 2 Conversion from high voltage to low voltage

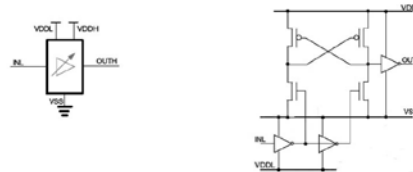


Fig. 3 Conversion from low voltage to high voltage

Output signals of power gating area are uncertain during power gating aiming at Power Gating technology. The uncertain state can lead to internal current of the load unit, thereby leading to unwanted power consumption. Isolation cells are inserted on output signals in the power gating area to realize isolation to uncertain state. Isolation cell can be divided into Yuxing or Huoxing structures according to different clamping values.

4.2 Power-Gating cell, Retention-Register and Always-on cell

Power-Gating Cell (also called MTCMOS) is required to realize power-on and power-off of power supply aiming at Power Gating technology. Disconnection power supply (VDD) or ground (VSS) connection can be selected to realize Power-Gating, these two Power-Gating Cells are referred to as Header-Switch and Footer-Switch vividly.

In Power Gating module, it may be required that register should lock the data before cut-off data or recover the locked data after power supply is connected. Special cell Retention - register is required. It has two power supplies, one is used for operation power consumption when module power supply is not disconnected, and the other is used for power consumption during module Power Gating. It also has two control signals for saving and restoration, they are used for controlling to lock or recover data.

Long-term work of some signal lines and logics is also required in power gating module, such as MTCMOS unit control signal line, Retention-register save/restore control signal, isolation cell control signals, etc. Additional special unit is required in order to achieve the function, and it is called always-on cell.

4.3 PG library preparation

Logical library (db library) for realization of UPF process is also provided with PG (Power&Ground) information in addition to these above-mentioned special units. The following information about PG is required compared with traditional process:

- pg_pin name, pg_pin types (such as primary, backup, etc.);
- Corresponding relation between each signal pin and pg_pin;
- Definition of power_down_function in each output signal pin;
- Voltage value of each pg-pin;

Tools can automatically complete connection of power network, power gating circuit verification, integration and optimization based on power state list in UPF, output of netlist verification with PG information, etc. according to description in UPF with the above information. The direct advantage includes more complete, simpler and more automatic flow.

4.4 Description of integrated circuit design intent with UPF

UPF contains all descriptions about low power design intent, such as: relatively independent power supply modules; power supply or ground in each power supply module; description of on-off

mode and control if power gating module is available, all working modes of each power supply (working voltage is shut off or not); special unit planning etc.

In UPF, all power domains should be defined. Top power domain should be firstly set. Two power domains of PD_1 and PD_2 can be described then. Then, power networks in each power domain should be described clearly according to power partition topology. Names of power cords in each domain and connection relationship with chip original power input port should be defined in details.

If Power Gating module is contained in the design, PD_1 and PD_2 cell should be defined in UPF for describing power supply input and output of the cell as well as connection of the control signal. If on-off module is available in the integrated circuit, the description of inserting isolation unit when the turn-off power supply module is turned off also should be increased in order to handle the stability of signal output after module shutoff functionally. In UPF, there is a very important part, namely description of Power State Table, and it is hereinafter referred to as PST, namely description of the working modes of all power supplies. The tool can be used for judging whether special cell should be inserted among all power supply modules with the table.

5. Conclusion

Low power consumption flow of Synopsys based on UPF standards is utilized, which is beneficial for reaching consistency, simplicity and consistency on description of low power design intention in the whole design flow (from front end to rear end and validation). Verification functions in all aspects are provided, thereby greatly improving the efficiency of design realization, and guaranteeing the correctness of design.

How to describe low power intention in own design by UPF is increased for design implementation engineer when UPF flow is compared with traditional flow. Low consumption design can be automatically realized by tools according to constraints in UPF. Many tools may be applied for implementation and verification. In traditional flow, each tool has own independent low power design commands, it is difficult to guarantee the consistency of descriptions among all tools. The problem can be completely solved with UPF. Uniform UPF file is used in all tools for obtaining consistent low power consumption design requirements. In addition, tools can be automatically inserted according to UPF description during front-end integration aiming at special cells for low power consumption design, such as isolation cells and Level Shifters. MTCMOS is inserted and connected in rear-end realization tools. Complex power connection, control signal connection and other steps prone to error in the whole process are automatically realized according to UPF description. The operation is simple and convenient with high accuracy.

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