High-speed and Huge-capacity Data Cache System Based on FPGA

Fei Gao [a,] *, Wenge Chang, and Xiangyang Li

National University of Defense Technology, Changsha 410073, China

[a] gaofeihit@qq.com

Abstract. Aiming at the high-speed and huge-capacity data cache and transmission caused by real-time signal processor for high-resolution SAR, this paper presents a design for the high-speed and huge-capacity data acquisition system based on DDR3 SDRAM and RapidIO. Data cache is realized by MIG3.92 IP core in Xilinx Virtex_6 series FPGA. Data Transmission is realized by RapidIO IP core and GTX. The testing results show that the maximum write rate of DDR3 memory is 3120MB/s and the transmission rate of RapidIO interface is 1800 MB/s.

Keywords: Cache; High-speed; Huge-capacity; DDR3; RapidIO.

1. Introduction

A data processing system of high-resolution SAR includes ultra-high-speed data acquisition module and real-time processing module. A/D of high sampling rate produces four channels high-speed source synchronous signals. The signals were achieved series-parallel converting by using ISERDES1 and transferred to the real-time processing module. The signal real-time receiving process involves the high-speed and huge-capacity data cache and transmission.

DDR3 memory can storage data on the rising edge and falling edge of the clock with the advantages of high integration, fast reading and writing speed, cheap price and so on.DDR3 meets the requirements of high sampling frequency data storage. RapidIO is a high speed point-to-point interconnect bus architecture based on packet switched interconnection architecture, is an open technology standard interconnect designed to meet the future demand for high performance embedded system. The maximum transfer speed of RapidIO channel is 5 Gbps. RapidIO meets the requirements of high sampling frequency data transmission. This paper adopts DDR3 and RapidIO to design the high-speed and huge-capacity data cache and transmission. The design of data cache based on USER INTERFACE is determined. Combining with the timing request of USER INTERFACE, the read and write control state machine is designed. At the same time, the design of high speed data transmission based on RapidIO 2.2 is proposed. The experimental results show that the write rate of DDR3 is 31200MB/s and the read rate of DDR3 is 6400MB/s. The stable transmission speed of RapidIO is 1800MB/s.

2. DDR3 SDRAM controller

Memory Interface Generator (MIG) is the Virtex-6 FPGA memory interface solutions core. The IP core includes a user interface, DDR3 controller and physical layer interface. USER INTERFACE is the connection mode provided by MIG IP core, connecting user design and memory controller. The characteristics of USER INTERFACE are follow:

- Buffers read and write data
- Reorders read return data to match the request order
- Presents a flat address space and translates it to the addressing required by the SDRAM.

USER INTERFACE meets the needs of ultra-high-speed data acquisition system, so the design connects users' design and memory controller by it. The overall program of DDR3 controller is shown the Fig.1.

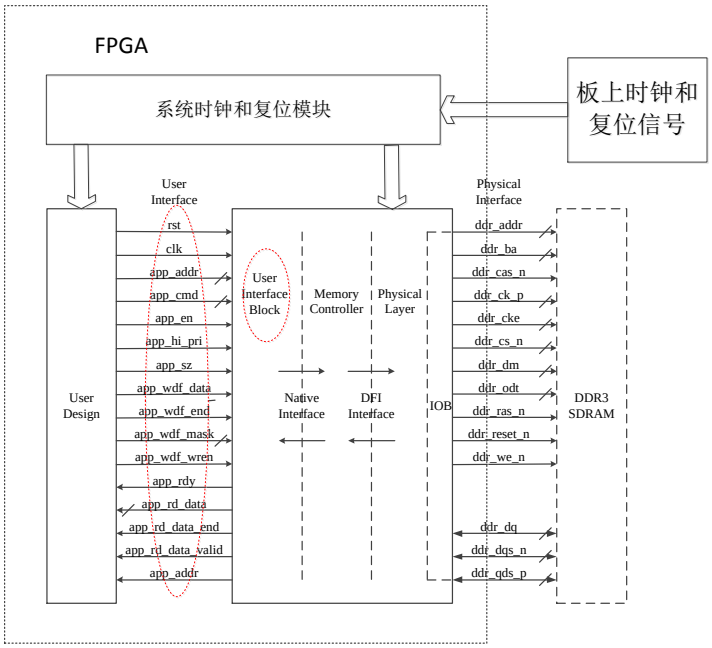

Fig.1 DDR3 controller

The user interface design is the core of the DDR3 controller, which mainly includes two parts.The user interface includes the write data access and the reading data access. The UI interface write timing is shown in Figure 2, and the UI read timing is shown in Figure 3.

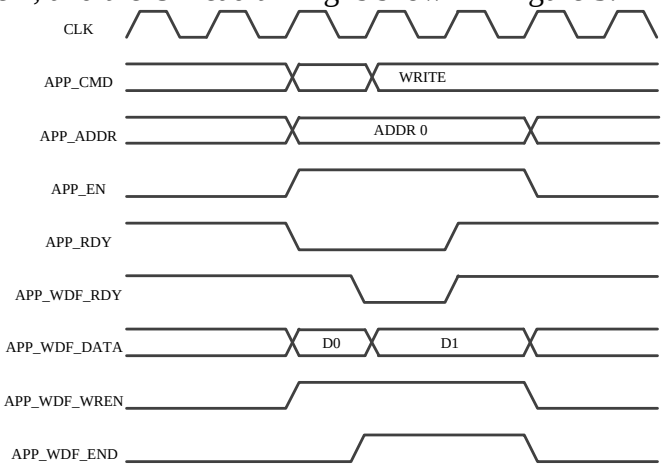

Fig. 2 UI Interface Write Timing Diagram

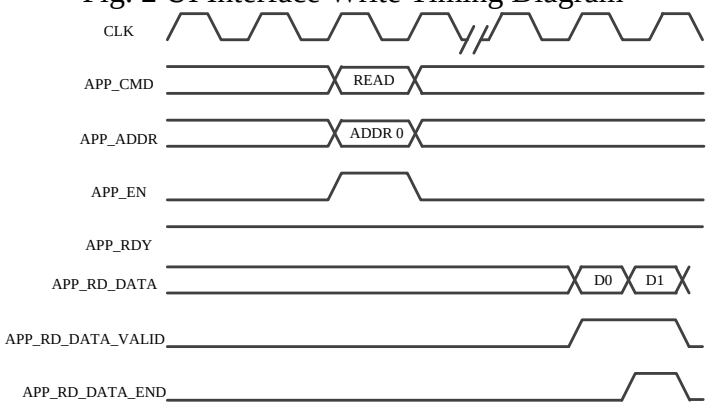

Fig. 3 UI Read Timing Diagram

Mixed-mode clock managers (MMCM) generates different clock signals. The input time clock is 100MHz. MMCM generates 200MHz reference clock and 400MHz working clock.DDR3 works in double data rate mode and the data width of four DDR3 is 64bits.So the theoretical transmission rate of DDR3 is 6400MB/s.

$$\frac{400MHz*2*64bits}{8}=6400MB/s=6.25GB/s$$

In order to reduce the difficulty of user timing, User interface clock is half of DDR working clock. User interface works in single data rate mode. The data transmission rates of user interface and DDR3 are the same. So, the data width of user interface is 4 times as much as the data width of DDR3. Input-output data and user interface work in different clock domains. So a FIFO is needed to cache data and convert clock. The concrete structure is shown in Figure 4.

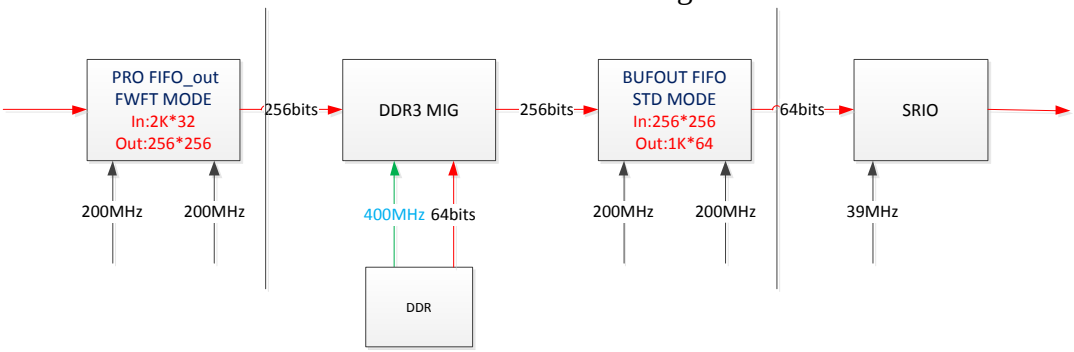

Fig. 4 Data Processing Flow

3. High Speed Data Transmission Circuit

The RapidIO is a high speed point-to-point interconnect bus architecture based on packet switched interconnection architecture. In practical applications, the speed of RapidIO interface is a core of data transmission circuit. The interface speed depends on the version of RapidIO, data width and Link speed selection. RapidIO 2.2 standard has already reached 6.25Gbps by single channel at present. In Xilinx Virtex-6 FPGA, the software design and hardware interface of RapidIO are independent of each other. The RapidIO IP core is the software architecture and GTX is the hardware configuration. The design of high speed data transmission circuit is shown in Figure 5.

The physical layer (PHY) is used to adjust link, initialize, and carry out the protocol, including insert the cyclical redundancy check (CRC) and confirm identifier to the packet output. PHY includes flow Controller, packet delineation and error reporting. PHY manages the link by 8B/10B code (K code) and coding efficiency is 80%. So the theoretical maximum of 5Gbps channel becomes 4Gbps.

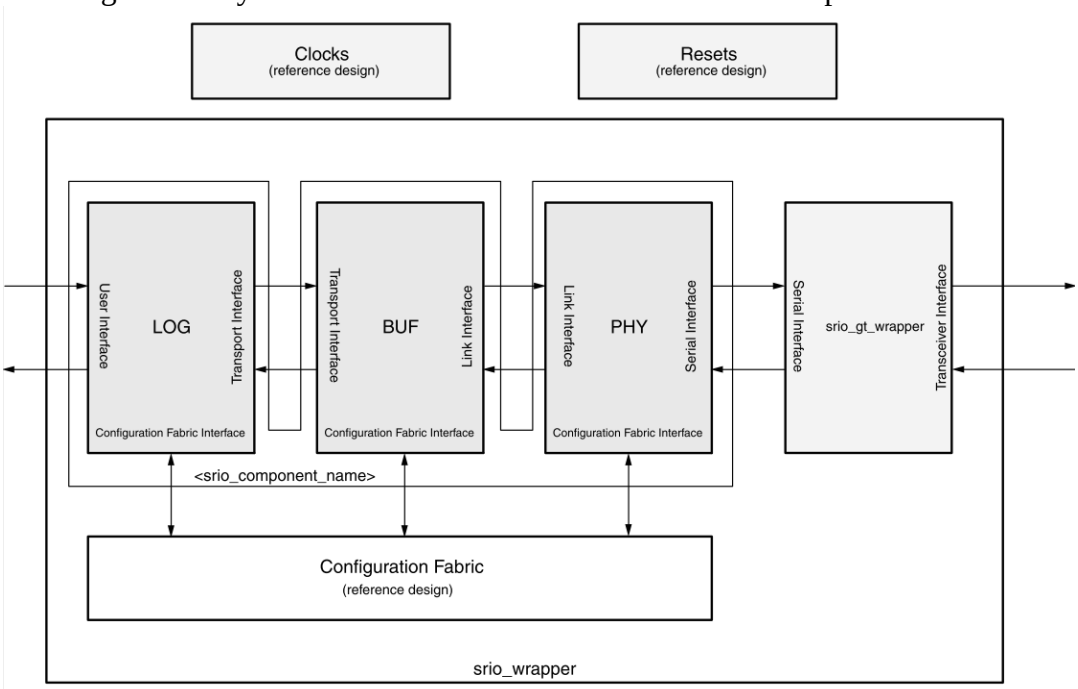

Fig. 5 Virtex_6 SRIO

4. Performance Test of Data Cache and Transmission

The performance test platform of data cache and transmission is shown as Fig.6. Virtex-6 Xilinx series XC6VLX240T chip is used as the main controller. The high speed data cache consists of 4 K4B2G1646C-HCH9 DDR3 chips.

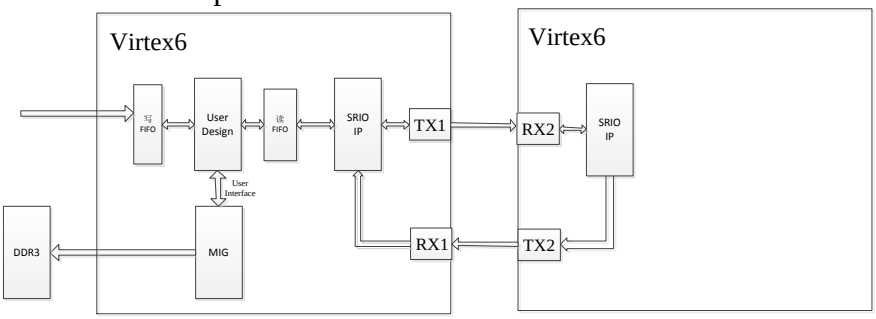

Fig. 6 Test Platform of Data Cache and Transmission

4.1 Performance Test of data cache

The FPGA platform of design is a complete SAR system, we did the online debug to correct the design errors with Xilinx Chipscope. The user clock is 200MHz. The data amount is 8K bytes. The data width is 256bits. The test results of data writing is shown in figure 7.

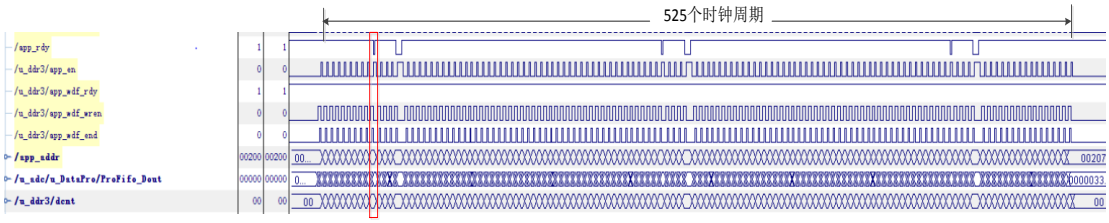

Fig. 7 Data Writing

As can be seen from figure, the controller writes data to the DDR3 when the address system and data system are in accordance with the time sequence. SELF REFRESH Operation appears on the red line. Other commands cannot be operated in SELF REFRESH Operation. The data writing spares 525 clock cycles .The write rate is 31200MB/s.

$$\frac{200MHz*8KB}{525}=3120MB/\mathrm{s}$$

The test results of data reading is shown in figure 8.The data reading spares 257 clock cycles. The read rate is 6400MB/s.

$$\frac{200MHz*8KB}{257}=6400MB/\mathrm{s}$$

The data from DDR3 is transmitted to the back-end real-time processing module by RapidIO. In order to ensure that the process does not appear data blocking, the read rate of DDR3 must be higher than writer rate of RapidIO. A FIFO is needed to match rate. The capacity is 32KB .The input data width is 256bits and the output data width is 64bits.The read rate drops to 1600MB/s.

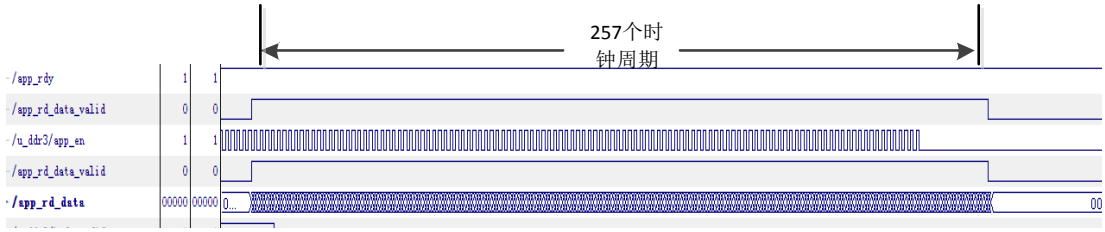

Fig. 8 Data Reading

4.2 Performance Test of data transmission

The GTX interface channel rate is configured to 5Gbps and the transmission mode is set to 4x mode by the RapidIO IP core. The test results of data writing is shown in figure 9.When the amount of data is low, the actual transmission rate of RapidIO is much lower than the theoretical value. The reason is that a large part of time is spent in packet packing and unpacking. With the amount of

transmission data increasing, the actual transmission efficiency is increasing. The stable transmission speed is 1800MB/s.

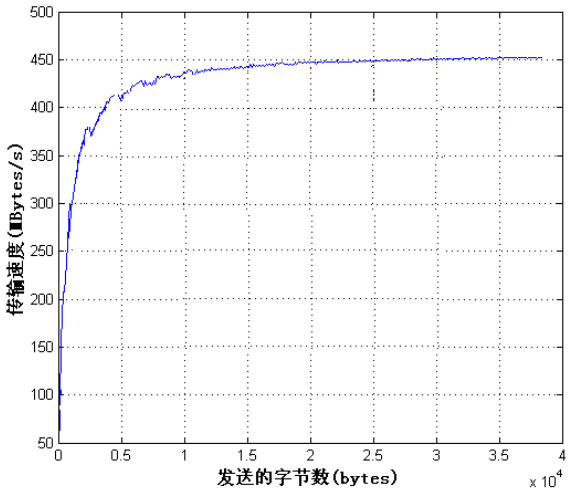

Fig. 9 Transmission Speed of RapidIO

5. Conclusion

According to a high-resolution SAR signal processing system requirements, this paper presents a design for the High-speed and Huge-capacity data acquisition system based on DDR3 SDRAM and RapidIO. The design of data cache based on USER INTERFACE is determined. Combining with the timing request of USER INTERFACE, the read and write control state machine is designed. At the same time, the design of high speed data transmission based on RapidIO 2.2 is proposed. The experimental results show that the write rate of DDR3 is 31200 MB/s and the read rate of DDR3 is 6400MB/s. The stable transmission speed of RapidIO is 1800 MB/s. At present, this design has been applied to the engineering practice.

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