Development of Full-waveform Acquisition Device in High Power Electrical Transmitter

Juan Wang [a], Shengli Hou [b*] and Shengquan Zhang [c]

School of Geophysics and Information Technology, China University of Geosciences (Beijing), Beijing 100083, China

[a]604649528@qq.com, [b]356455536@qq.com, [c]quanquan902000@163.com

Abstract. Multi-channel Transient Electromagnetic method (MTEM) is a method with the ability to detect deep and precisely. It is a hot topic in the electro-magnetic field. This thesis works on designing a full-waveform recorder for monitoring high-power electrical transmitter. It is composed with hardware and software, which has high precision and low noise level. The data of voltage and current collected by the recorder can be restored and transmitted to the receivers in real time. The whole device is reliable and stable through long-time tests.

Keywords: Multi-transient electromagnetic method; High power electrical transmitter; Current collection; Acquisition device.

1. Introduction

MTEM was initially mentioned up by David Wright who came from the University of Edinburgh and Anton Ziolkowski in 2001 [1]. Compared with the traditional TEM (Transient Electromagnetic Method), the operating mode of MTEM are as follows: (1) it uses the grounded-wire-source mode; (2) it uses the source signal PRBS; (3) observation method: array; (4) it depends on a transmitter to send off the signal and receive the signal in array way. The arrayal moves along with the surveying line [2]. The center point between the source and receiver is used as the measuring point of MTEM detection. (5) It measures earth pulse reflecting voltage and emission current simultaneously.

There are still some problems with the domestic MTEM to be solved. For example: the incorrect quartz clock synchronization; emission current is descending off the array track due to vibration; it is not able to adjust the time of emission current descending automatically; there is still a problem to develop the matching detector; the capacity of resisting disturbance needs to be improved; interior noise existing in the apparatus [3]. Therefore the developing directions presently are as follows: the transmitted waveform of the apparatus needs to be changed; better techniques are needed for noise suppression; better techniques for the clock synchronization; develop the techniques of Weak Signal Detection; making a correlation between the apparatus and installations. In order to improve the technical shortcomings of the domestic MTEM apparatus, we have designed a recording device for the voltage and electric current to monitor the high-power MTEM transmitter. The full waveform recording device is able to gain the four-way signal acquisition precisely from the voltage and electric current in low speed or high speed respectively. The stable and reliable data acquisition could be achieved in the long-term machine test process.

2. Integrated Design

The integral structure of the full waveform voltage and current is represented in the Figure 1, which is composed of hardware and software. Hardware is mainly composed of the front end conditioning circuit, data acquisition circuit, high-accuracy atomic clock circuit, the feed circuit and the governor circuit, whose core parts are mainly, FPGA and SDRAM memory. The software consists of FPGA (VHDL included) program, USB chip firmware, MSP430 taming atomic clock program and PC (upper computer).

The conditioning circuit of voltage analog board divides and then follows the transmitter's high voltage, making the signal magnitude satisfy the input range of the analog-to-digital converter while the high voltage going into the collector board; another part of conditioning circuit's output goes

through the comparing unit, shifting it into the LVCMOS voltage level to send to the IO of the FPGA for frequency measurement. There are two ways of collecting circuitry respectively on the current and voltage analog boards: 32KSPS low-speed sampling and 40MSPS high-speed sampling. After the digital value is converted by the analog to digital converter, it will go through light couple isolation, and then it will be sent to process in FPGA.

Comparing with conditioning circuit of the voltage board, the current board's is different in the ways that firstly the transmitter's large current is changed into the voltage signals through the current diverter for measurement, and then the weak voltage signal getting through the high-gain and high bandwidth amplifying circuit is conditioned and sent to the back-end converter.

The major function of the governor circuit made of the FPGA and SDRAM memories are as follows: to integrate the digital value gaining from the low-speed voltage, low-speed current, high-speed voltage and high-speed current circuit; to measure frequency of the square wave coming out from the comparing unit; and the collected data is sent to the PC to make the real-time display and storage.

The Bluetooth and 485 modules are mainly used to send off the peak value, frequency value and time information of the current and voltage signal. The module of the high-accuracy atomic clock provides the highly-stable clock signal and GPS pulse information for the signal collection. The lithium battery and NI-MH battery in the feed circuit provides the low output ripple and high-performance electric source for each module of the circuit.

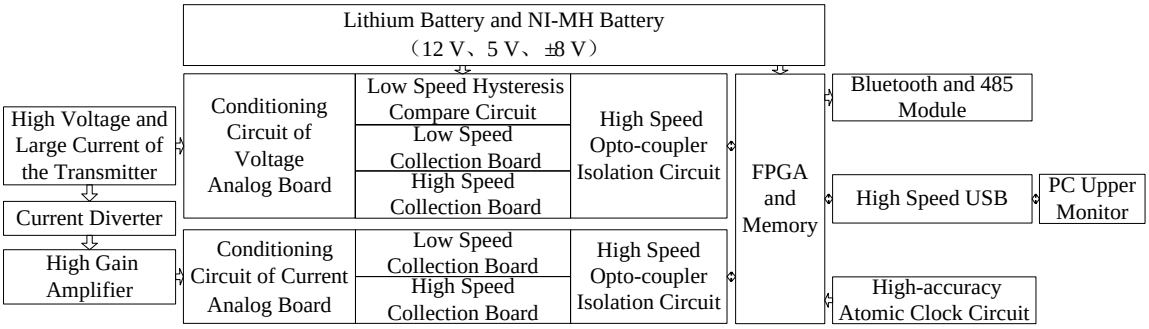

Fig. 1 The overall design framework regarding the voltage and current full waveform recording device

3. The Design of Hardware Circuit

3.1 The Design for the Front End Conditioning Circuit based on High-Speed Optocoupler.

The front end conditioning circuit of the full waveform recording device can be made of two parts: the conditioning circuit from the voltage collection part and the conditioning circuit from the current collection part.

The conditioning circuit's structure from the voltage collection part is represented in Figure 2.As soon as the voltage signal from the transmitter gets through the voltage separation, it gets through the follow and conditioning process, eventually being sent into the analog to digital converter, while the collector board and the master control board use the high speed photo coupler as the isolation for the electrical signal. Besides, hysteresis compare circuit is used for signal shaping and frequency measurement [4].

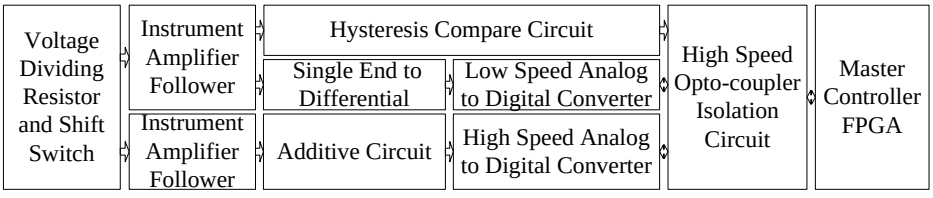

Fig. 2 The structure framework about the voltage acquisition based on the high speed optocoupler digital isolation technology

The conditioning circuit's structure from the current collection part is represented in Figure 3.What is different from the voltage collection parts is that this part doesn't do the repeat measurement of frequency so that it doesn't need the hysteresis compare circuit. The large electrical signal from the transmitter gets through the current-voltage transfer and then it goes into the high bandwidth and high magnification mu-circuit.

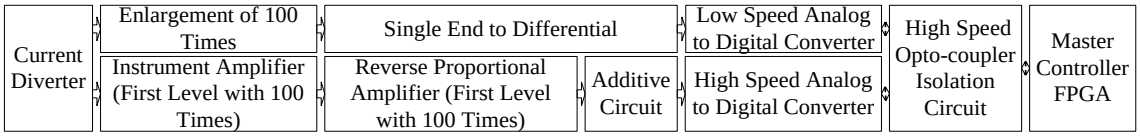

Fig. 3 The structure framework about the electric current acquisition based on the high speed optocoupler digital isolation technology

3.2 High-Speed and Low-speed Acquisition Circuit Design.

The Low-Speed Acquisition section uses 32 KSPS sampling rate. This analog-to digital converter is a high-accuracy 24 bits Δ-Σ type which supports three working modes: High-Speed Mode, High-Accuracy Mode and Low-Power Consumption Mode. In order to satisfy the whole machine's signal-to-noise rate standard, the Δ-Σ type analog-to digital converter does the acquisition under the High-Accuracy Mode. The High-Accuracy reference source from Linear Technology Corporation is used as the external reference voltage. Analog power supply uses the PI type LC filter to make sure the power supply's pureness and does the wiring for analog and digital part separately, and links the common ground with a single 0 Ohm resistor.

The High-Speed Acquisition section uses 40MSPS sampling rate, this analog-to digital converter is a 12 bits pipe-lined one and its sampling rate can be up to 65MSPS, meanwhile its bandwidth can reach 750MHz. The non-harmonic disturbance dynamic range is 85dB when the input signal is 31MHz. The falling edge of the electrical prospecting signal often contains lots of shallow layer information. In order to keep these information, this design uses the low-speed rate to gain the full waveform while at the same time designs other high-speed acquisition circuit. Compared to the electrical transmitter's microsecond-level transition time, the allowance space of 40MSPS sampling rate is big enough.

3.3 Design of the FPGA Main Control Circuit.

The major functions of MTEM transmitter voltage and current full waveform recording device are the control of collection and data transfer, which are mainly finished by the main control FPGA circuit (the control core of the recording device). The main control circuit is composed of the master core board and the main connecting panel.

The master core board mainly consists of the FPGA (Cyclone the third generation one from ALTERA Company) and some external memory. The memory is made of SDRAM and serial FLASH these two types of memories, of which the SDRAM is used as the data buffering for the low-speed acquisition and the serial FLASH is used as the FPGA configuration program's memory. The main control connecting panel is mainly used to give the core panel electricity supply, which contains the high-speed USB chip and 485 chip, moreover the connecting board is also used to connect current and used as the voltage analog board, clock board and Bluetooth module.

There are two methods of downloading the main control FPGA chip [5]: one is to put the SRAM configuration files inside FPGA through JTAG link, however, the internal logic vanishes as the FPGA runs out of power; other way is to put the SRAM configuration files into the serial FLASH through JTAG link, and the FPGA chip's configuration procedure can be finished once the power is on again. The design of the FPGA main control circuit is shown in Figure 4.

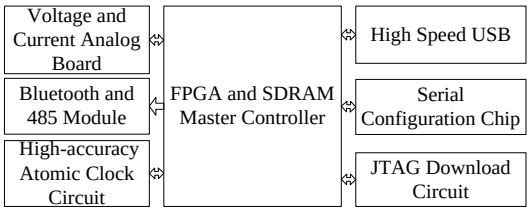

Fig. 4 The structure framework regarding the FPGA main control circuit

4. The Design of the Software Program

4.1 The Design of the VHDL Program of FPGA.

There are several modules in the VHDL program of FPGA: the clock and resetting module, the ADC acquisition and control module, the serial sending and receiving module, the SDRAM buffer controller module, high-speed edge acquisition and control module, USB control and convey module and the equal-precision frequency measurement module. Each module mainly monitors each time sequence with the state machine, different combinational and sequential logic circuit in order to gain the real-time data acquisition and stable transmission [6].

The clock and resetting module uses the PLL module built-in FPGA to make the input 50 MHz clock division and multiplier adjusting to get the fixed value.

The ADC acquisition and control module is able to do the data reading of high-speed and low-speed analog-to-digital converter, each point of collected data insert into the data head which is made of the time stamps including the GPS time sequence and pulse per second. And finally write these data into the FIFO to make it readable for the downstream data flow control module.

The serial sending and receiving module is used to receive the time sequence sending from the GPS module. COM(Cluster Communication Port) transmittal is used to transfer the information regarding the peak signal value, frequency and time to 485 module and Bluetooth through upper computer ,and then all of these information will be sent to the electrical receiver through the 485 bus or the Bluetooth.

In order to gain the waveform on both side of transition edge, firstly transition edge needs to be gained. Originally this design used the data which are gained from the high-speed analog-to-digital converter, but after the actual measurement we realized that if there is some noise adding to the waveform, it is difficult to judge the transition edge signal. Then we've made some change that the trigger signal on the edge is changed into the output signal of the hysteresis comparison circuit on the electric platen in order to make sure that the transition edge is in the middle of the data flow. There is about 2000 sampling points before and after the edge through the high speed signal acquisition being put into the FIFO. After 4096 points being gathered, they will be transmitted to the upper computer through the USB transmission module, and then after 1 second, it will be go on the next round's judge and transmission.

The collected high speed voltage, high speed current, low speed voltage, low speed current signal and the frequency data are being sent to the relative endpoint in the USB chip respectively. As for the downstream data sent from the upper computer to the USB chip, this module asks for the FIFO empty and full mark individually and read the data timely and send them to the serial port module.

4.2 Design Regarding the USB Chip Firmware.

Used as the bridge between the lower machine and upper monitor, USB chip plays an important role [7]. Its internal buffer area is divided into four endpoints. Once the upstream endpoints in the buffer area of the upper endpoint are full of storage, PC upper monitor have to move it away otherwise the buffer area will be too full to lose the data; that is to say that, once the buffer area of downstream endpoint is full, the FPGA in the lower machine have to move it away otherwise the buffer area will be too full to lost the data.

The firmware program mainly modifies the BULKLOOP's set routine program on the official website and adds the necessary configuration which this project needs. The company's official website CYPRESS has already built the framework for the USB transmission, what you only need to do is to fill the function code in the function.

4.3 The Design Regarding the PC Upper Monitor Program.

The upper monitor is on the Visual Studio platform which a project is using the C #window program to be built [8]. The program is mainly made of the main window program, sub window program and a user-defined function. In the main window program, each channel's read and write function are entrusted to relative 8 threads by processing the sampling or interception from the data flag bit and the channel type so that the data points used to describe the waveform can be obtained and open the 4 thread drawing program to do the drawing. The generic function uses the USB device's

each channel to encapsulate one type according to port address. And the sub window program is used to open the saved data file and playback waveform.

5. The Comprehensive Test of the Full Waveform Recording Device

After finished the hardware and software design and debugging for the full waveform recording device, each module will have a performance and function test. Through the analysis of the test data, we can judge that the accuracy of the high speed acquisition and low-speed acquisition can reach ±1‰, the overall signal-to-noise rate is better than 90 dB; the data transmission between the lower machine FPGA and the upper monitor PC is accurate without errors; the real-time display and repeated display of the upper monitor function all meet requirements; the data acquisition in long term's overall test is stable and reliable.

6. Summary

In this essay, according to the actual demand, we develop a full waveform voltage and current recording device to apply to the MTEM transmitter. The overall test result shows that the hardware and software design of the system is correct. The recording system for the data of voltage and current is provided with many advantages such as the high-accuracy, edge details are abundant and low-noise. These data can be gained timely and transmitted to the receiver so that the correlation decoding be carried out.

References

[1]. G. Q. Xue, X. Li, Q. Y. Di. The progress of TEM in theory and application. Progress in Geophysics, 2007, 22(4): 1195-1200.

[2]. D. Wright, A. Ziolkowski, B. Hobbs. Hydrocarbon detection and monitoring with a multicomponent transient electromagnetic (MTEM) survey. The Leading Edge, 2002, 21 (9): 852-864.

[3]. A. Gregory, Deep transient electromagnetic soundings with a grounded source over near-surface conductors. Geophysical Journal International, 1989, 98 (3): 587-601.

[4]. T. C. Xun. Research of Correction and Effect of Transimitting Waveform on the Transient Electromagnetic Response. Chongqing University, 2008.

[5]. Q. S. Zhang, M. Y. Deng, K. P. Yang. Application of SOPC on High-precision Geoelectric Data Acquisition System. Geoscience, 2012, 26 (6): 1306-1311.

[6]. S. Pan, J. Y. Huang. EDA technology and VHDL (Second Edition).Beijing: Tsinghua University Press, 2007.

[7]. K. Zhang. Comparison of USB Controlling Chip's Performance and Its Development. OME Information, 2008, 30 (20): 26-29.

[8]. M. H. Liu, M. Z. Jin, H. H. Yan. An C# Component Model Based on Visual Studio. NET. Computer Engineering and Applications, 2003, 39 (30): 20-22.