The Design and Implementation of IP Cores in CCD Image Optical Fiber Transmission System

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Abstract. To overcome the complex logic in CCD image optical fiber transmission system, this paper introduces the concept of MicroBlaze soft processor and IP cores in the system, and transmit data through AXI bus. With the advantage of IP core in SOPC system, this design optimize the CCD image optical fiber transmission system effectively.

Introduction

CCD image data can achieve long-distance transmission through CCD image optical transmission system. With the system can be used in more and more occasions, it's particularly important to monitor and ensure the quality of the image. With logic design, the image data can be converted from serial to parallel or from parallel to serial conveniently, however, it's complex to interact with the monitoring system in this way. To solve the problem, this paper introduces the MicroBlaze processor and IP core, and high-level language can be programmed on the embedded system. Combing it with traditional logic design, not only that the image data can be operated easily, but also that the transmission system can exchange information with monitoring system easily, and the quality of the CCD image can be ensured effectively.

Currently, SOPC which is based on FPGA has been widely used in telecommunications, industrial, medical and other environments. SOPC combines hardware platforms which contains processor, memory, and IP cores with software systems into a programmable FPGA chip, and has the characteristics of flexibility and portability.

System overall design

The overall architecture of MicroBlaze processor and IP cores in CCD image optical fiber transmission system is shown in Fig. 1.

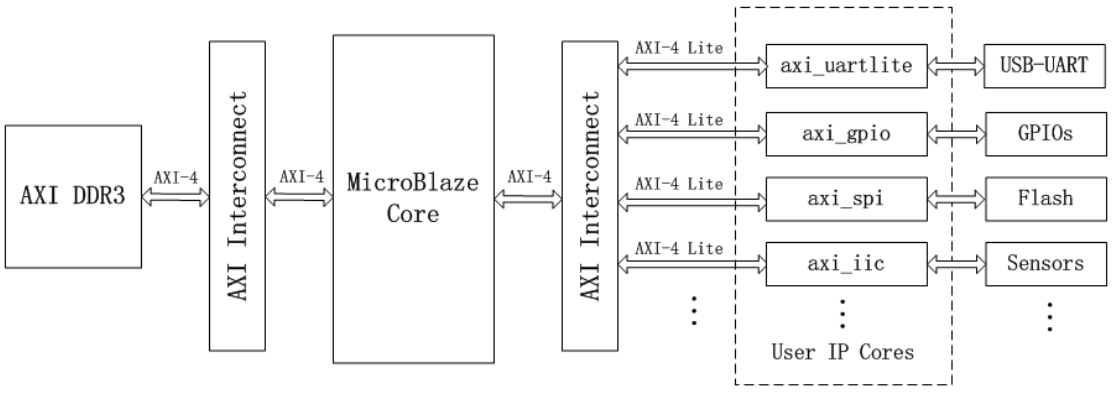

Fig. 1 Overall system architecture

This system mainly consists of three parts: MicroBlaze processor is responsible for data processing and computing; user IP cores can achieve interface function to external, and are added to

AXI interface module as AXI-4 Lite peripherals; AXI bus interface is responsible for data transmission between MicroBlaze and user IP cores.

MicroBlaze Processor

As the core of embedded system, the processor plays a crucial role. MicroBlaze is a kind of soft processor core with 32-bit RISC and Harvard architecture, and provides a rich instruction set for embedded applications. Based on MicroBlaze soft processor, it's flexible to choose memory, interface and peripheral devices to achieve the desired embedded system with minimal resources on a single FPGA.

The internal structure of MicroBlaze processor is shown in Fig. 2.

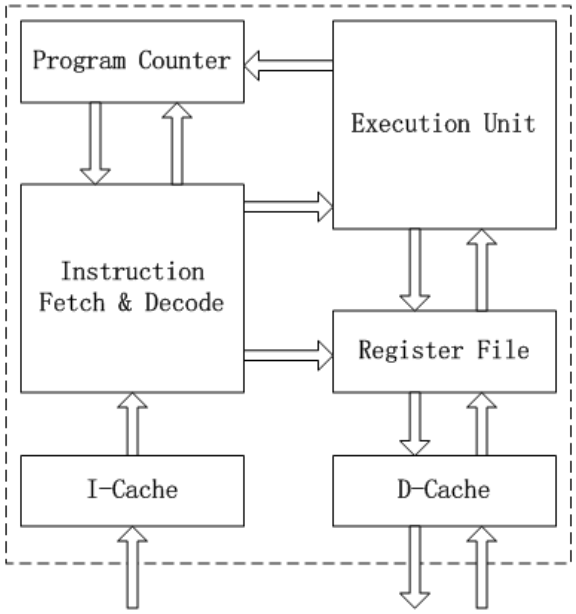

Fig. 2 The internal structure of MicroBlaze processor

The unit of I-Cache in MicroBlaze reads instruction information from the instruction bus interface, D-Cache exchange data with the data bus interface, the size of the caches above can be adjusted from 2KB to 64KB. The Instruction Fetch & Decode unit obtains instruction from the I-Cache and decodes it, then sends the instruction decoded to the Program Counter unit, Execution Unit, Register File. The Program Counter reads instructions and data from the Instruction Fetch & Decode unit and Execution Unit respectively, and feedback to the Instruction Fetch & Decode unit. Register File unit, which consists of 32*32 bit registers and special registers, reads instructions from the Instruction Fetch & Decode unit, and exchanges data with the Execution Unit and D-Cache respectively. The Execution Unit can execute addition, subtraction, shift, logical operations and floating-point operations, and the result is sent to the Register File and the Program Counter unit.

AXI4-Lite Bus Protocol

AXI4-Lite bus protocol is lightweight AXI4 protocol for simple, low-capacity memory-mapped communication, such as communication between control and status registers. AXI4-Lite includes five different channels: write address channel, write data channel, write response channel, read address channel and read data channel. These five channels ensure bidirectional transmission of data between the master device and the slave devices.

When data is transferred from master device to slave device, the master device writes address and control information to slave device through write address channel firstly, then the slave device returns response information through write response channel. The master device starts writes data to slave device through write data channel after the transmission channel is established.

The difference between read data and write data in AXI4-Lite protocol is that there is no response channel in read data process, and the direction of data flow is opposite. Since AXI4-Lite protocol provides independent data and address channel for read and write process, continuous bidirectional data transmission is allowed.

User Defined IP Core Design

Traditional CCD image fiber transmission system uses hardware logic to realize the image transmission and interact with the host computer, which causes the system logic is complicated. To solve this problem, encapsulate the interfaces to user defined IP cores, use software approach to communicate with host computer by MicroBlaze processor. With MicroBlaze and IP cores, the complexity of the system is reduced, flexibility and reusability are increased. This paper takes axi_uartlite and axi_iic core for example to show the structure of user defined IP core.

User IP Core: axi_uartlite

To ensure the quality of image transmission, the test system is needed to monitor transfer data in real time via the serial port. The traditional serial port implemented by hardware logic is not flexible enough, but the serial encapsulated into IP core can be implemented simply, and has high flexibility. The internal structure of axi_uartlite IP core is shown in Fig. 3.

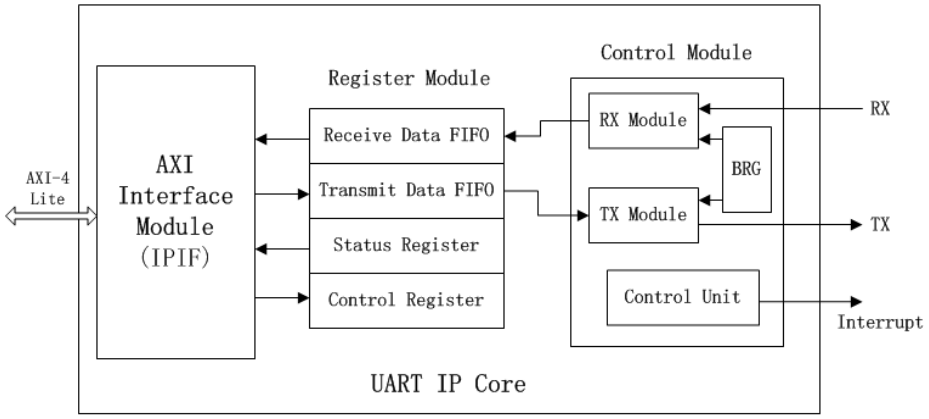

Fig. 3 The internal structure of axi_uartlite

As shown in Fig. 3, IPIF module on the one hand communicates with MicroBlaze through AXI4-Lite protocol, on the other hand transfers data with the user registers. Register Module includes 16 bits Control Register, Status Register and a pair of Transmit/Receive Data FIFOs, and they can communicate with AXI bus via the IPIF module. The Control Module comprises: RX Module, receives data from external and sends to the Receive Data FIFO; TX Module, obtains data from the Transmit Data FIFO and sends to the external; BRG, generate baud rate to the RX/TX Module; Control Unit, provides the necessary interrupt information for the system.

User IP Core: axi_iic

External environment such as temperature and humidity can affect the quality of CCD image transmission too, therefore sensors are needed to monitor the external environment, and most of these sensors use IIC interface to transfer data. Fig. 4 shows the internal structure of axi_iic IP core.

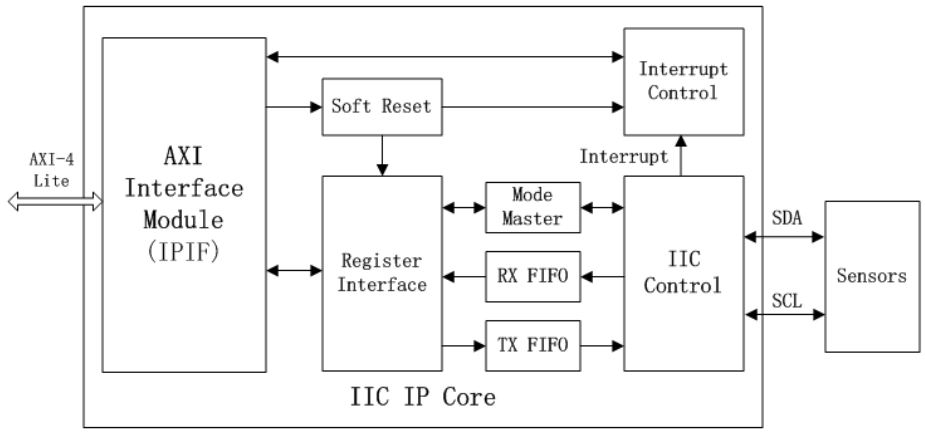

Fig. 4 The internal structure of axi_iic

The IPIF module in axi_iic IP core exchanges data with Register Interface and Interrupt Control. Register Interface module includes control and status registers, receives data from RX FIFO and sends data to TX FIFO. Contrary to the TX FIFO, the RX FIFO stores data flow from IIC interface to

MicroBlaze processor temporarily. The Mode Master and IIC Control module are combined to decide the IP core work in master or slave mode dynamically, and IIC Control module exchanges information with external sensors directly. The Interrupt Control module generates interrupt information for IP core according to the soft reset and control information in different circumstances.

IP Core Encapsulation

User defined IP cores can be designed and encapsulated with the Create and Import Peripheral wizard that EDK software provided, the encapsulation process is shown in Fig. 5.

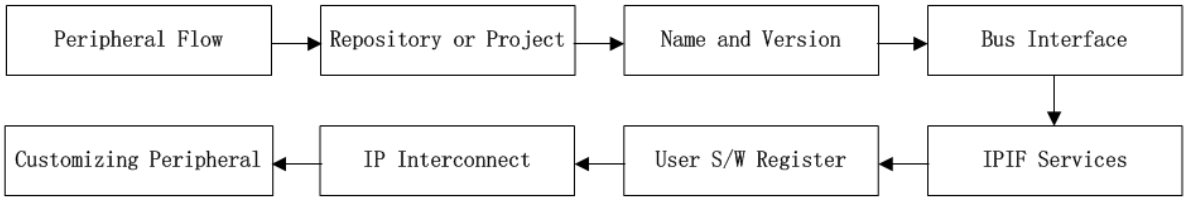

Fig. 5 The encapsulation process of user defined IP core

In the process of encapsulating user defined IP core, the kind of bus interface, such as AXI4, AXI4-Lite, AXI4-Stream, PLB and FSL, can be selected in the Bus Interface procedure. That determines the IP cores are mounted on which kind of bus. The IPIF should be configured in IPIF Services procedure. IPIF module is independent of the user interface, and provides many optional features, including software registers, the user address range, FIFOs, software reset, interrupt support. The signals that IPIC supported can be configured in IP Interconnect procedure and these signals can be transmitted between the user logic and AXI bus.

Summary

In this paper, MicroBlaze and IP cores are used to replace the logic design in CCD image optical fiber transmission system. The IP core design based on SOPC has the features of flexibility, portability and short development cycle. This design not only guarantees the quality of CCD image transmission, but also reduces the complexity of the system, and also has the reference significance to other similar systems.

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