Synchronization of JESD204B-based ADCs

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Keywords: JESD204B, deterministic latency, synchronization, Radar system

Abstract. With the rapid development of radarsignal processing systems, a great demand of high-speed communication is required. JESD204B interface has become an outstanding solution for ADC-related data transmission, and has been widely applied. However, the synchronization of multiply JESD204B-based ADCs has been a challenge because of the special feature such as deterministic latency. In this paper, we design a data acquisition system integrated two JESD204B-based ADCs, and proposed a general and flexible synchronization method based on FPGA, by using and controlling deterministic latency. As is validated by the practical measurements, the method can maintain a phase difference between the two 2.5Gbps ADCs from 17ps to 22ps stably, for the signals of frequencies less than 1.8GHz.

Introduction

Conventionally, CMOS or LVDS is employed to transmit the acquired data between ADC with the processing unit, such as FPGA, but recently the JESD204B interface has change this situation, and become more and more accepted. Rather than CMOS and LVDS, the JESD204B interface offers several advantages in terms of speed, size, and cost. Its data transfer rate can reach up to 12.5Gbps, and this provides sufficient bandwidth to keep balance with the ever increasing ADC sampling rate[1].

In high-complexity signal processing system designs, multiple analog-to-digital converters(ADC) are commonly integrated to obtain larger dynamic ranges and high performance, and their synchronization determines the overall performance. As for the JESD204B interface, it introduces a deterministic latency for each converter in the system, and this helps to make multi-ADCs synchronized.

In previous work, multiple ADCs of JESD204B interface was used in downlink data reception and processing of the digital phased-array radar, and the two ADCs inside the AD9250 was synthesized by using deterministic latency[2]. In another paper [3], the two ADCs inside the JESD204B-based AD9680 was also implemented by using deterministic latency, and the phase difference was limited to 45ps. The previous work makes it available for synchronizing two ADCs inside a chip, but the synchronization becomes more challenging when it comes to independent ADCs.

In this paper, we design data acquisition system by integrating two independent ADC9625 provided by Analog Devices, Inc.(ADI) company, which is a 12-bit converter and compatible with JESD204B. As the other termination, we use a Xilinx Vertex-7 FPGA as the controller and receiver, whose development kit is Vivado2015.4. By using and controlling the deterministic latency, we propose a general and flexible synchronization method based on FPGA. The method is validated by the practical measurements, and it can control the phase difference between the two ADC9625 less than 20ps for various frequencies, under 2.5Gbps condition.
The rest paper is arranged as follows. The deterministic latency of the JESD204B is introduced in section II. Our method for synchronizing multiple ADCs is described in section III. The section IV concludes the paper.

**Deterministic Latency of JESD204B**

Deterministic latency across the JESD204B link is defined by the time it takes serial data to propagate from the parallel framed data input at the transmitter to the parallel de-framed data output at the receiver. As illustrated in Fig.1, it includes three components: the delay from the transmitter to the output, the spatial routing delay, and the receiver delay from the input to the de-framer. Different ADCs have their own unique deterministic latency, even in the same system.

![Fig.1 Illustration of Deterministic Latency](image1.png)

There are three subclasses of the JESD204B protocol, and they have different deterministic latency definitions. Here we chose the paper-used subclass 1 for further demonstration.

**The Principle of Deterministic Latency for Subclass 1.** Subclass 1 supports deterministic latency by using a SYSREF signal as the reference. As illustrated in Fig.2, the frame clock and multi-frame clock are aligned internally to the SYSREF edge.

![Fig.2 Samples are aligned after the clock latches a SYSREF edge](image2.png)

Subclass 1 defines a receiver buffer, and its release time is referenced by the SYSREF signal. The buffer enables the receiver to deskew the samples of early arrival of data to match with the latest arrival of data by using buffer delay [4], as illustrated in Fig.3. As a result, the multi-frames of different links are aligned to the multi-frame clock by using buffer delay within the receiver.

![Fig.3 The function of the receiver buffer](image3.png)
Here the period of aforementioned SYSREF must be multiple of the period of local multi-frame clock (LMFC), and it should be synchronous with the device clock and be accurately controlled to make sure an fixed clock edge.

**The Implementation of Deterministic Latency for subclass 1.** Although the deterministic latency offers a good way for synchronization, the deterministic latency uncertainty (DLU) limits its implement, and need some compensations. The DLU means the LMFC skew and it includes two parts: the first is the un-controlled distribution skew of the device clocks (DCLK) in the system, and the other is SYSREF distribution skew (DS\textsubscript{SYSREF}), which means the time difference between the earliest arriving SYSREF and the last one.

![Fig.4 Deterministic Latency Uncertainty](image)

Since the JESD204B-based ADCs usually work at a very high rate, its setup and hold time requirements become challenging [5]. To meet this, each device in the JESD204B system should have its own SYSREF/DCLK pair, and their phase delay should be adjusted to ensure the timing [6], as illustrated in Fig 5. The SYSREF can be delayed in fixed increments, and a phase that makes the SYSREF edge near to middle of the valid window is recommended to ensure the minimum DLU.

![Fig.5 Adjustment of the SYSREF phase delay to minimum DLU](image)

**Design of JESD204B-based ADCs Synchronization**

With the demand of data acquisition precision and high sampling rate, the data acquisition system integrating FPGA and ADC has become a mainstream of the industry design. In the section, we elaborate our data acquisition system with FPGAs and ADCs integrated, and demonstrate our method for synchronizing multiply JESD204B-based ADCs.

**Demonstration of the Data Acquisition System.** The data acquisition system is comprised of mother and daughter boards for versatility and flexibility considerations. The mother board implements controlling, processing, and data handing out, and the daughter board acquires and transfers external signals. They are connected through the high-pin count (HPC) connector (400 pins), which supports up to 10Gbps per lane.

As illustrated in Fig 6 (left), the Xilinx Virtex-7 in the mother board communicates with daughter board including the JESD204B interface through two HPC connectors. The daughter board includes a clock driver AD9520 from ADI and a convert AD9625. The former offers clock for the latter, and
the latter communicates with Virtex-7 FPGA through JESD204B interface, as illustrated in Fig.6 (right). The AD9625 is a 12-bit monolithic ADC that can operate at conversion rate up to 2.5Gsps.

![Fig.6 Design of the mother board and the daughter board](image)

**Design and Implement of the Synchronization based on FPGA.** We design a JESD204B controller based on FPGA, and it includes three modules: high-speed serial receiving module, deterministic latency signal generation module, and the configuration module, as is illustrated in Fig.7. The high-speed serial receiving module receives data through Gigabit Transceiver (GTX), the deterministic latency signal generation module is used to generate the SYSREF signal, and the configuration module configures the setup parameters to AD9520, AD9625, and FPGA GTX core.

![Fig.7 Implementation of multiple ADCs synchronized sampling based on FPGA](image)

We use 8 lanes in our design, and we determined other parameters, according to the specification of AD9625[7]. By setting the ADC sampling rate as maximum 2.5Gsps, we can calculate the multi-frame clock as 19.53125MHz, and here we set the SYSREF frequency equal to the multi-frame clock as 19.53125MHz. To minimize the DLU, we adjust the SYSREF phase delay by HMC988, which is capable of adjusting SYSREF phase delay in 20ps steps.

**The result of multiple synchronized ADCs based on JESD204B.** The test setup of multiple synchronized ADCs is shown in Fig 8. A signal generator is used to provide sampled signal of 12dBm and the other provides a 10MHz reference clock of 10dBm. To eliminate the influence of transmission between the two daughter boards, the length of transmission lane are kept equal and
the signal should divide by a power divider. To ensure the accuracy and robustness of the achieved phase difference of the two ADCs, we tested several incremental frequencies from 10MHz to 1800MHz, when the AD9625 working in 2.5Gsps.

Using FFT to calculate the imaginary part and the real part of the signal, the signal phase is the arctangent of the ratio of the imaginary part and the real part. We analyze the data by Matlab and the result of phase difference value between the two ADCs is shown in Fig.9.

Fig.9 the phase difference value between the two ADCs

**Conclusion**

To satisfy the demand of high sampling rate and high transmission rate, we design a data acquisition system integrated two JESD204B-based ADCs. To implement the synchronization of the ADCs, we proposed a general and flexible synchronization method based on FPGA, by using and controlling deterministic latency. Through the measurements and data analysis, it is conclude that the phase difference value between the two 2.5Gsps ADCs is well controlled from 17ps to 22ps stably, for the signals of frequencies less than 1.8GHz. The result shows that the design of multiple ADCs synchronized has a high performance for Radar systems.

**Acknowledgement**

This work was supported by the Chang Jiang Scholars Programme (Grant No.T2012122) and the Hundred Leading Talent Project of Beijing Science and Technology (Grant No. Z141101001514005).

**References**


