Research on the Genetic Algorithm and the Convex Optimization Theory and the Applications on the Large Scale Integrated Circuit Design

Zhenbang Xu, Hong Shi

Jiangsu Vocational College of Information Technology, Wuxi, Jangsu 214153, China

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Abstract. In this literature article, we conduct research on genetic algorithm and convex optimization theory and the applications on the large scale integrated circuit design. Integrated circuit test system's main function is to test the microprocessor, semiconductor memory circuit and a variety of dedicated circuit and the high performance test system can complete function test and the dc parameters test, ac parameters. Basic test system structure consists of computer subsystem and the testing and measuring subsystem. Under this basis, we propose the novel perspective of the large scale integrated circuit design pattern that will promote the VSLI industry in China.

1. Introduction

   With the rapid development of basic system integration and processing technology, VLSI test has become a more and more difficult problems. Advanced technology can make people at a reasonable cost of rapid design and manufacture of complex circuits, with the loss of the product cost, increasing proportion of the total cost of testing [1-2].

   As through integrated circuit design and production process of general integrated circuit testing has become an important support for the development of integrated circuit industry as is a high and new technology will bring the improvement of product quality and reduce costs, advanced test process and test methods that can effectively control the product quality in the production of each link and cost. In order to control the cost engineers need of continuous specification testing process, improvement and combination of various test methods. The figure one shows the concepts.
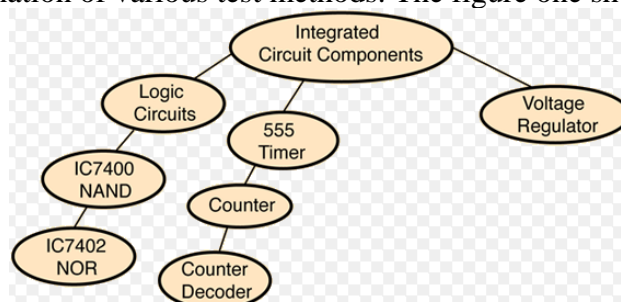

Fig. 1 The Procedures of the Large Scale Integrated Circuit Design

   As for the general testing of the VLSI, the principles could be summarized as the follows. (1) Test pattern generation method. In general production stage, as much as possible to prevent defective or the malfunction of the chip into the market, and need to check them, it needs to be inspired by testers use tester on chip, and analyzes its response to determine that whether there is a fault chip. (2) The memory test. Functional memory tests including chip level respectively, array level and board level test. In order to make the test economy, that chip level test memory fault model must be adopted. A memory array test is used to test the chip selection and control logic. You must test the memory array as refresh memory board test logic, error detection and error correction logic, plate selector hardware, storage controller. (3) IDDQ test. IDDQ said stationary state power current, called the static power current, or leakage current. This current is called IDDQ testing. IDDQ test is a test of originates from physical defects, but also a part of the reliability test.

   Large scale integrated circuit integration density is higher and higher, can be produced on a silicon chip has tens of thousands of collective tube and now many chip has been included in the multiple, complex system, therefore, called it a very large scale integrated circuit system. In this research paper,

to deal with the mentioned challenges, we conduct research on the genetic algorithm and the convex optimization theory and the applications on the large scale integrated circuit design.

2.   The Proposed Framework

2.1 Genetic Algorithm.

Genetic algorithm is a professor at the University of Michigan John Holland in the late 1960 s is put forward for the first time rooted in Darwin's theory of evolution, the group of Mendelian genetics and that species selection theory and the Weizmann. In genetic algorithm, the crossover operator by simulating the hybrid process of biological nature of individual crossover operation, and continuously produces new individuals, increase diversity of population, expanding the scope of the optimization, so as to make the genetic algorithm has strong search ability, can say crossover operator in genetic algorithm extended space, and achieve the global optimal process plays a vital role [3].
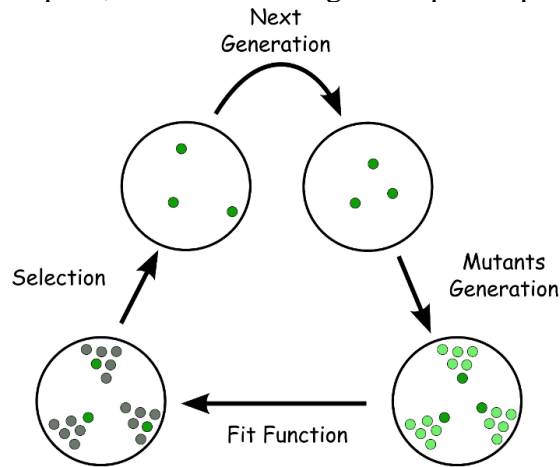

Fig. 2 The Systematic Description of the Genetic Algorithm

As a kind of adaptive global optimization algorithm, the probability of genetic algorithm to search for the ultimate orientation, its features are as follows. (1) Genetic algorithm is a kind of self-learning and adaptive ability of intelligent algorithm. Traditional algorithm design requires all properties and characteristics of the problem in advance and according to different characteristics to adopt different means to solve the problem. (2) Using a fitness function to complete the intermediate solution vector of evaluation and to guide the search direction of optimization of function is not continuous and that differentiable request. (3) Handle object itself is not a problem of parameters of genetic algorithm, but the code set parameters. (4) It is a kind of parallel algorithm. Its each iteration based on the population rather than a single complete solution space of the search process, thus has a degree of parallelism.

Simple genetic algorithm because of the crossover and mutation probability can't reflect evolution process, thus easy to appear the phenomenon of premature or random roaming as formula one.

$$P_{content} = f_{\max} - f_{general} \qquad (1)$$

Based on the stability of the algorithm in order to solve the contradiction between the convergence speed and global convergence, this paper proposes a new improved genetic algorithm. We can think so, GA started from the starting point in the solution space search the optimal solution of problem and the TS is using memory function of the pioneers in the search process, they are solve various question the success of the application show that using both to solve complex problems is valuable.

If is sparse distributed among individuals or rarely, as they are not a stable focus groups, they are considered to reduce the probability, they are also the probability of crossover and mutation also want to reduce, or may produce a lot of unnecessary interference. On the contrary, if the middle area of the individual lot or more concentrated distribution, more stable, shows the group, they are considered probability also increases accordingly, i.e., increase the area selection probability values.

2.2 Convex Optimization Theory.

Since the 1960 s, people have already realized the excellent characteristics of convex optimization; In the 70s, the convex analysis obtained the very good development as emerged in the 90s, deal with

new algorithms and the software convex optimization problem all optimization problems reflects the convexity, watershed is not linear and the nonlinear optimization problems, but the convexity and the convexity that can be reflected from the figure two [4-5].
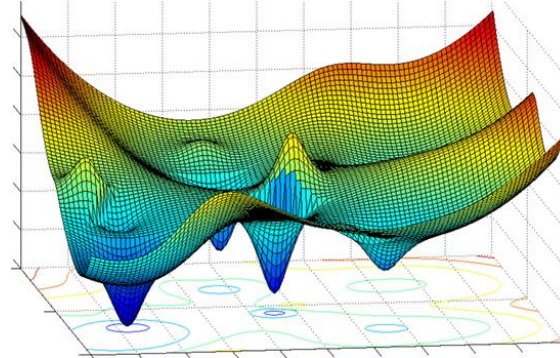

Fig. 3 The Visualized Demonstration of the Convex Optimization Theory

To solve these problems, we must break through the traditional theory of limit of sampling method, can reduce the sampling rate while still in the guarantee the important information in the signal is not lost. Therefore, the issues could be transferred into the formula 2.

$$L(x, y) = f(x) + \sum_{i=1}^{n} y_i c_i(x) \tag{2}$$

Use of original signal sparse feature in the transform domain, the signal can be under-sampling or dimension reduction, and from less than the observed value of original signal dimension accurately reconstruct the original signal that compared with convex optimization method and greedy iteration method, non-convex optimization method on the target vector of sparse have stronger constraints.

2.3 Large Scale Integrated Circuit.

The layout of the integrated circuit layout before actual in simulating, its purpose is to make every component can be placed on the most appropriate location, to predict the connection and length of the internal signal lines, confirm element driving ability, and estimate the chip size, to control cost, so that the gap between layout planning and layout results to a minimum.

Current analog signal test is mainly based on DSP simulation tester is applied based on the DSP function test vector, but is faced with a large number of test vectors and very long test time, therefore, based on the fault model of basic analog circuit fault simulation and automatic test vector generation method in industry gradually be accepted as the test based on the model of analog signals were offered the opportunity to shorten the number of tests which can be used as supplement of traditional method. As devices in different stages of development design and the manufacturing process, different device under test, different technology conditions, testing technology can be divided into many types.

- Ac parameters test. Ac parameters transistor devices under test to measure temporal relations during the transition state. Its purpose is to ensure that the device state transitions within the prescribed time as the feedback performance evaluation.
- A functional test. Test pattern is the important way for testing device function is good or bad, a good test graphics has high fault coverage and short testing time, to effectively test failure and the device being tested process defects. So the quality of the test circuit depends on the accuracy of test vector.
- The output load capacity test. It is used for the inspection device in the permitted load capacity under the condition of noise. The test to ensure the device to the expected under certain load current output level [6-7].
- The power supply current test. Used to test the device within the prescribed voltage under the condition of maximum current power consumption. It is whether the detection device defects in one of the most effective way and it can be divided into static power consumption test and the dynamic power consumption test.

2.4 Integrated Circuit Design Optimization.

Compared with the other IC CAD tools that map circuit extraction also seem to be very immature. Although many map circuit extraction method and general extraction apparatus were mentioned, but compared with the modern circuit design ability, map circuit extraction is ragged [8].

Competition of digital circuit design is to point to two events occur at the same time under the condition of the circuit can't distinguish the sequence of that events resulting in a circuit work result uncertainty. Such as the establishment of the trigger time change the data input port, so the output of the trigger value cannot be determined. Accordingly, we propose the listed suggestions for the core steps. (1) With the constant improvement of the scale of integrated circuits, as map graphic number increase rapidly. If by scattered or in front of block, it must be to map processing, all calls to the unit is to map each of the geometry processing, requires a lot of machines. (2) Block extraction circuit is divided into blocks, each single extraction in memory while then each piece of combined extracting sub-circuits. Because the block is arbitrary, so always can guarantee each in current machine full run, and hence effectively in the limited memory space to realize the electrical network and its parameter extraction. (3) Of the circuit to extract main advantage is a unit of repeated calls are usually only are extracted that only deals with one unit at a time, reducing the demand for space, greatly improved the extraction rate and at the same time, to extract the netlist to keep the original hierarchical structure design that provides a convenient for web table after work.

3. Conclusion

In this paper, we conduct research on genetic algorithm and the convex optimization theory and the applications on the large scale integrated circuit design. Information technology is the core technology of the national economy, it services to national economy each domain microelectronics technology is the key to the information technology. Integrated circuit as the core of microelectronics technology, integrated circuit industry to improve the foundation of the innovation of information technology and competition ability has a very important role and the integrated circuit is the foundation of the whole information industry and information society is the embodiment of the high and new technology. In the future, more research will be down for modification.

Acknowledgements

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