STM32 microcontroller core ECG acquisition Conditioning System

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Abstract. In order to achieve real-time monitoring of ECG, the paper design a set of ECG data acquisition system based STM32 microcontroller conditioning. Design of the system is divided into hardware and software in two parts: hardware including ECG acquisition, preamplifier, bandpass filter and amplifier, band-stop filter and level lifting circuit, 50Hz double trap circuit T and A / D acquisition LCD display circuit, the software part of the main STM32 module is configured to implement serial communication, use of assembly language programming, using modular structure. This design affordable, high stability, has some practical value.

Introduction

ECG (ECG) is generated when the human heart beats bioelectrical different locations on the body surface of physiological changes in the signal, it can reflect the speed of the beating human heart, in order to determine the health status[1]. With the improvement of people's living standards, heart disease has become the number one killer threat to human health, with a hidden disease, the rapid development of high-risk life and other characteristics[2], which ECG has always been an important topic in the medical field.

With the advances in modern technology, the use of computer-based signal detection system equipment to obtain ECG information to assist physicians in order to become the development trend of medical consultation. Therefore, a need for a capable and PC ECG detection system data communication[3]. This paper presents a kind of STM32 microcontroller core, through the use of technology to collect the body's front-end ECG, and by AD620, OP2177 as a signal conditioning system which enables the measured ECG is normal, noise is effectively suppressed, stable circuit performance.

System Design Overview

ECG Acquisition conditioning system including analog acquisition and digital processing in two parts, the design collection of human ECG electrodes and through AgCI three leadwires ECG acquisition line, through the preamplifier circuit, the band-pass filter circuit, 50Hz double T notch wave and then through the main amplifier and the level of the lifting circuit ECG amplitude control in the STM32's A / D acquisition range, STM32 by timer setting A / D sampling frequency, by the way mean filtering the resulting figures signal processing, and finally depicted on color electrocardiogram shape[4], Overall system block diagram shown in Figure 1.

Hardware Design

control module circuit design

STM32F103VE SCM control module is the core of the controller, the MCU STMicroelectronics ST peninsula is produced by 32 high-performance, low cost and low power Enhanced MCU, its core uses ARM's latest Cortex-M3 architecture produced the maximum operating frequency of 72MHz, 521kB of program memory, 64kB of RAM, 8 timer / counters, two watchdog and a real-time clock RTC, on-chip communication interface has two I2C, 3 SPI, 5 USART , a USB, a CAN, a SDIO, and integrated three ADC and a DAC, has a 100-pin, 80 general-purpose I / O ports[5] . Master SCM LQFP100, Figure 2 is LQFP100 pin arrangement.

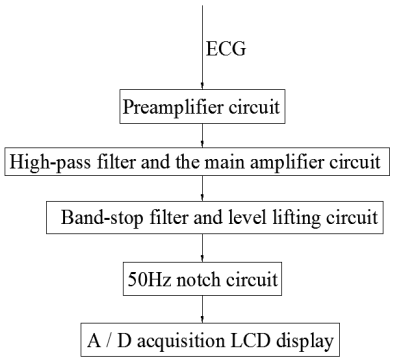

Figure 1 Overall system block diagram

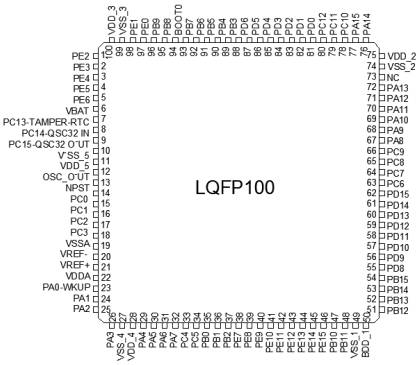

Figure 2 STM32F103VE microcontroller pin map

Design preamplifier

Preamplifier is the key to ECG data collection. It is the ECG amplifier for amplifying the first stage, due to the ECG signal amplitude input is very low, and mix some interference signal, so the main function is to filter preamplifier common mode interference signals, while the ECG differential mode a certain degree of amplification. To achieve this purpose, the design uses instrumentation amplifier AD620 as a pre-amplifier having an input paranoid low current, low noise, high accuracy and low power consumption characteristics[6] , to fully meet the requirements of the design characteristics, its circuit diagram shown in Figure 3.

band-pass filter and a main amplifier

The system design using integrated operational amplifier OP2177 constituting the high-gain band-pass filter, and its high precision amplification for weak ECG acquisition. OP2177 internal dual op amp cascade to ensure the differential input stage tends to symmetry, which has a very low offset voltage and drift, reducing noise; while OP2177 low input bias current, and thus a very low power consumption.

Even without the use of external compensation circuit, OP2177 for large capacitive load (> 1000pF) still has a stable output voltage of 30V when the power amplifier consumes less than 15mW. Protection OP2177 input signal amplifier is a high-precision double by internal 500-ohm series resistor to achieve, when the input signal level is higher than the supply voltage can ensure that the input signal is not inverted.

So we can use the above advantages OP2177 to build amplification and filtering circuit design of the system. Meanwhile, the human ECG signal bandwidth of about 100Hz, band energy is concentrated in the 0.02 ~ 150Hz, noise and harmonic components of the ECG signal energy major existing cardiac, cardiovascular disease and related peripherals brought no more than 300Hz. The OP2177 internal dual op amp IC are designed as active low-pass and high-pass filter, a combination of the pass band at least 0.01 ~ 500Hz band-pass filter, shown in Figure 4.

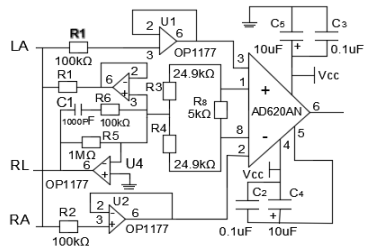

Figure 3 Preamplifier circuit diagram

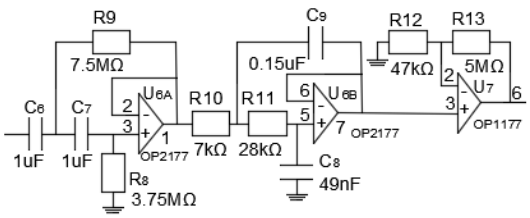

Figure 4 Bandpass filtering and amplifying circuit diagram of the main

band-stop filter and level-up circuit

To filter out 50Hz frequency interference, the system circuit joined the band-stop filter. System output is 0-5V, due to the positive and negative logic filter uses an AC signal, so to meet the design output requirements, output filter must be level upgrade, designed to enhance the range of at least half the maximum output amplitude. Figure 4 is the use of integrated operational amplifier 0P27, R11, R12, R13 form a reverse adder circuit, the output signal will be coupled with a bias voltage from the bias circuit R9, RI0 component on the circuit can be adjusted during commissioning R10 produce appropriate bias voltage. Adjust the scope of the design bias voltage is 0-10V (VCC = 12V), the input

signal filter thus inverting adder regulated bias voltage is output -5V-0. R14, R15, OP27 constituting an inverter, to ensure that the final output signal within the voltage range of 0-5V. The system design of band-stop filter with a high quality factor, so its filter bandwidth is narrow, the ECG detected with good inhibitory selectivity.

ECG normally collected after the amplifier has a negative level, while the converter during A / D conversion is defined minimum switching voltage is 0V, the ECG must be amplified in order to ensure the potential to enhance ECG signal in an A / D conversion by MSP430F149 negative level when distortion does not occur, and all were positive level analog to digital conversion. Its level-up circuit shown in Figure 5.

50Hz T Parallel band-stop filter design

Double T parallel 50Hz band-stop filter circuit essentially consists of two T-type high-pass filter and low-pass filters connected in parallel Figure 6 shows, the symmetrical design parameters to ensure the circuit has a good degree of zero drift suppression. The main role of this circuit is suppressed by ECG 50Hz frequency interference. The circuit cutoff center frequency of 50Hz, in order to improve the accuracy suppress and prevent occurrence frequency and elegant, using silver mica capacitor circuit design, resistance metal film resistors, the system design using error <0.1% metal film resistors, which makes the 50Hz power frequency interference signal attenuation circuit capacity can reach 60dB.

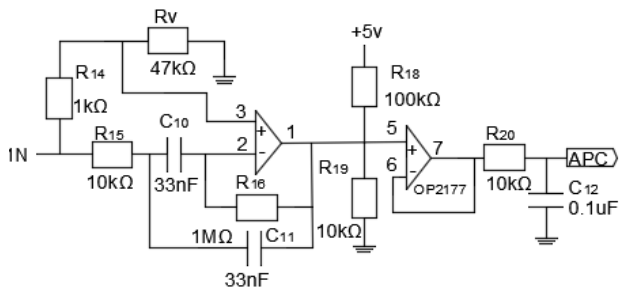

Figure 5 Bipolar level to the level of potential unipolar boosting circuit

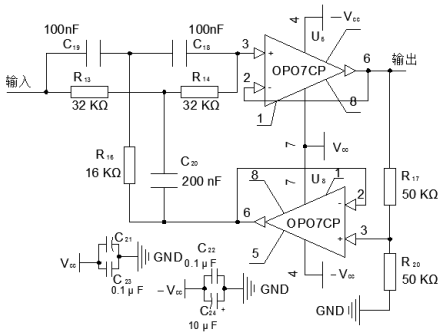

Figure 6 50HZ band stop filter

Software Process

The system software design is modular assembly language. After the system boot initialization, using the timer overflow into the signal acquisition mode, the ECG signal collected by the A / D conversion, data storage and processing, and finally to the display. Eventually on the color screen to describe point method to achieve the waveform obtained after the initial ECG signal is displayed in real time software control, namely accurate and fast. In addition, the host control data storage conversion and showed that various forms of data can show the way, to facilitate the detection by data analysis. Program flow shown in Figure 7.

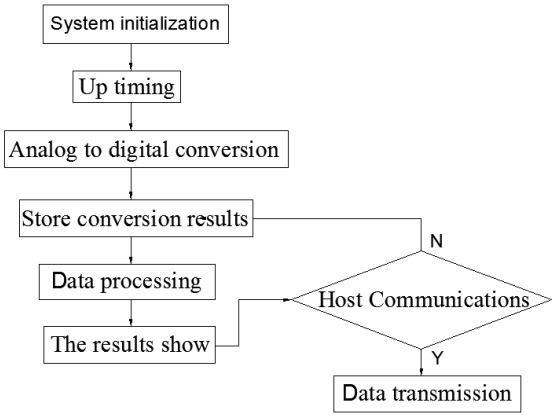

Figure 7 system software flow chart

Found Results

The system in the body by placing the left arm, right arm, right leg electrode sheet and three lead wire acquisition signal after a preamplifier circuit and STM32 chip processing, ECG waveform on the screen obtained 8 shown approximately between QRS peak shows 900ms, the patient can get the measured heart rate is about 67 beats / min, reflecting the real situation of the patient. Judging from the waveform monitor, the image can clearly reflect the basic electrical characteristics of the human heart, among which the PR and QT interval significantly, which P-wave, RP segment, QRS wave, ST segment and T wave have significant representation, can provide medical personnel provide basic care and diagnosis. Signal of 50Hz frequency interference has been significantly inhibited visible circuit design is successful.

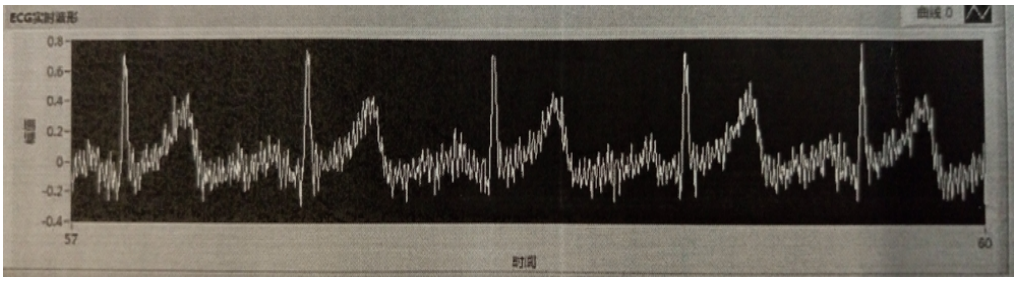

Figure 8 ECG crest

The system uses a preamplifier AD620, the instrumentation amplifier featuring low noise, high impedance characteristics, can well suppress the zero drift and common-mode signal, for weak ECG signal acquisition and amplification with high precision and transmission performance . Overall gain can reach nearly 30dB, the common mode signal rejection ratio> 97Db, the whole input impedance reached 180MΩ, the band in response 0.01Hz to 100Hz, completely covering normal and abnormal ECG frequency range to achieve the design requirements. Machine design using his right leg drive circuit and the common mode signal driving shield, combined with double T parallel band-stop filter design methods and level upgrade, effectively suppressed frequency interference signal, the quality factor raised to 5, to reduce the power consumption of the circuit.

The system uses the serial Flash memory chips AT45DB321 problem solving large-capacity data storage, the storage capacity of up to 30Mbit. Moreover host MSP430F149 SPI serial interface data Data flash memory for reading.

Conclusion

This design is based on STM32 as the control center for the faint of heart in AD620 signal acquisition and preamplifier to OP2177 signal processing and the main amplifier circuit, circuit performance is relatively stable and can effectively suppress noise and signal interference environment, measuring the output ECG waveform stable. Circuit design of the whole system is not complicated, high precision, and can basically meet the love of a heart to heart disease surveillance and home care. The experimental measurements show that the design of low cost, perfect function, simple operation, friendly interface, high degree of humanity, has a certain value.

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