Research on the Low Power and Low Voltage CMOS Integrated Circuit Design Patterns and Methodologies

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Abstract. This paper presents the novel research on the low power and low voltage CMOS integrated circuit design patterns and general methodologies. With the integrated circuit technology to the rapid development of the deep sub-micron and nanometer order of magnitude, how to reduce the power consumption of the integrated circuit has become equally important problem with speed, area, power consumption constraints to further improve the performance of the chip, and increase the cost of the integrated circuit. A high level of integration and the application of high-speed device, especially in today's mobile devices and battery power equipment of the large-scale promotion, makes the power dissipation problem is becoming more and more prominent. Our research combines the literature list of reviews to propose the novel implementation paradigm for better performance.

1. Introduction

The reliability of semiconductor devices in a large part of the way that is depends on the reliability design of the product. In the process of general product development, must be reasonably by means of reliability technology and the engineering design method can effectively improve the reliability of the product, to ensure the reliability of the products. Only in device design reliability basis to achieve high reliability of products. CMOS integrated circuit development up to now, traditional two-dimensional planar integration process has reached its integration density limit, in order to increase performance chip integration more transistors, it is necessary to increase the chip size, and chip size increased with the extension of basic global interconnect distance, the more the grim problem of interconnection to overcome interconnect bandwidth limitations, we must change design method. The advantage of the polycrystalline silicon integrated circuit and the design difficulty can be listed as follows.

- Due to the polycrystalline silicon is made up of different grain size and phase velocity of grain boundary structure characteristics, each of the thin film transistor threshold voltage that carrier mobility and series resistance, resulting in the output characteristics of polycrystalline silicon thin film transistor has a great deal of dispersion.
- Polycrystalline silicon and the monocrystalline silicon components they have their respective advantages, applicable to different aspects of monocrystalline silicon device is mainly used in high speed in the large scale integrated circuit, device belongs to the body as is prepared on the single crystal silicon.
- Some sensors and liquid crystal display pixel circuit and so on. In amorphous silicon or glass or electronics, flexible substrate preparation polycrystalline silicon devices very good choice.

CMOS circuit there is two main sources of general power: static power consumption and dynamic power consumption. Among them, the dynamic power consumption caused by short as circuit current power consumption and power consumption of the load capacitance, static power is mainly caused by the leakage power consumption. In the current source model in the design of the drive, the size of the reference current can affect the output signal swing. To reference current source circuit performance, and therefore, the demand is higher and higher, in order to prolong the service life of the battery at the same time while the benchmark current source should have lower power consumption.

Sampling data processing circuit is the sampling signal, as namely time discrete and continuous signal amplitude, it is a kind of discrete time circuit, so the basic unit is similar to the digital circuit, mainly the additive, delay, multiplication coefficient, differential and integral circuit, the input output

characteristics and tracing fan with the difference equation. But due to it being processed signal not quantitative, so won't produce quantization noise because of this primarily analog signal processing circuit, so in analog circuit. At present commonly used circuit voltage circuit, it is with the change of the voltage as the carrier of information, complete the processing of voltage variables. Current mode circuits based on the change of the current information carrier, complete the handling of the current variable. In the following figure one, we demonstrate the sample status.

Fig. 1 The Sample CMOS Integrated Circuit Design Methodology

2. Our Proposed Methodology

2.1 Integrated Circuit Design Patterns.

With the development of computer technology, people in the design process more with the aid of computer aided design. Mainly is the use of computer aided software for circuit diagram, map input and edit, also can used for simulating the stages in the process of design and simulation and then the CAD software also provides all kinds of basic circuit integration rule checking, greatly improving the integrated circuit design predictability and accuracy of the product.

Fig. 2 The Review of the Integrated Circuit Design Patterns

SOC is developed on the basis of the ASIC circuit, it is totally different from ASIC that has many unique advantages. (1) SOC is greatly reduces the cost of the whole machine: made up of the past with multiple pieces of IC system, as now becomes a SOC. (2) SOC significantly reduce the volume of the whole machine: this is the system manufacturer in the direction of further development, especially for portable computers, communications and multimedia products manufacturers more attractive. (3) SOC added functions: increased from single function to general multifunction, realize the function of a system, realized the high speed, high integration and low power consumption.

There are three different ways of SOC chip design as the first method called the dedicated system design method. System agreed upon the righteous system indicators, SOC chip should be adopted in IP module, such as general IP, dedicated IP designed by the chip makers. The second method is called

a partial integration means. System manufacturers dedicated circuit part of the SOC chip design. The third method called desktop integration means supply of all kinds of IP module companies provided to the electronic system, design the special circuit part, by an electronic system, and combined with outsourcing various IP complete SOC chip design.

2.2 The CMOS.

Operational amplifier is the most basic circuit of the analog integrated circuit unit its importance is known to all. The CMOS process is a kind of design by the use of low voltage operational amplifier, low power consumption with gain, the high stability, wide common-mode input range, low frequency, low power consumption, high power supply voltage rejection ratio and high common mode rejection ratio with the current driving ability. If really didn't have the function of negative feedback, I believe that the vast majority of amplifier circuit is not working well. But due to the introduction of the large loop negative feedback circuit, the speaker of counter electromotive force through feedback circuit and the input signal superposition, cause quality fuzzy, sharpness drops, so there are a part of the final stage of the power amplifier used without big loop negative feedback circuit, by trying to disconnect the negative feedback loop to remove the disadvantages brought by the large loop negative feedback.

Fig. 3 The Visualized Demonstration of the Operational Amplifier

The CMOS reference source in the basic starting point is the use of MOS tube in the threshold region saturated with gate leakage current source voltage characteristics of exponential relationship, create a has nothing to do with the power supply voltage is proportional to the absolute temperature of the reference voltage, it can provide a stable source of small benchmark. According to the electrical property of MOS transistor and the threshold area theory, the leakage source current is as follows.

$$I_{DS} \approx I_{D0} \beta \exp\left(\frac{V_{GB}}{mV_t}\right) \left[\exp\left(-\frac{V_{SB}}{V_t}\right) - \exp\left(-\frac{V_{DB}}{V_t}\right) \right] \quad (1)$$

Supply voltage can make other MOS tube in the saturated zone as the sliding sideways through the MOS tube current can be equalized as the formula 2.

$$I_{biasTerm} = \frac{V_t}{R} \frac{\beta_i}{\beta_d} \ln\left(\frac{\beta_b \beta_c}{\beta_a \beta_d}\right) \quad (2)$$

PMOS differential input stage with high input impedance, its input common-mode negative power supply voltage of low level can reach the following, and under the same conditions, using the PMOS differential input stage is better than using the NMOS differential input stage of noise performance. Because of PMOS differential input stage and level displacement static working current of the circuit is determined by the reference source of reference current, and push pull output stage of the size of the static working current and resistance of the resistance, therefore, as long as well to adjust the size of the various parameters that can make the op-amp circuit static work done very little electricity.

2.3 Power Consumption of the Integrated Circuit.

The realization of the low power integrated circuit is a comprehensive project, power consumption of the device, circuits and systems need to be considered at the same time optimization that need a compromise between performance and power consumption. The current international most advanced low power consumption chip solutions based on basic silicon CMOS technology, from the system implementation method, system architecture design, management technology, circuit structure and the power consumption CMOS device material, structure and process a multi-angle and multi-level

comprehensive optimization and compromise. But with integrated circuit into nanometer scale, and is suitable for the application of general low power CMOS technology platform caused by the leakage of MOSFET current increase, severe parasitic effects such as problem increasingly prominent, currently many low-power technology became the preliminary solution, it is difficult to fundamentally solve encountered in the development of integrated circuits power consumption limitation "problems, to some extent, affected the sustainable development of nanoscale integrated circuits.

Because in the design of the hardware design in the process of different levels has the different characteristics and different levels of dynamic power consumption optimization space also vary as the follows. (1) Timeout strategy. This is a kind of principle is the most simple, but it is also the most widely used technology. The timeout strategy with fixed timeout period can be divided into strategy and strategy of adaptive timeout two cases. (2) Prediction strategy. It through to the system request load history records were analyzed, and the equipment before entering the idle state can predict the equipment free time length, if free time is more than can be predicted energy saving, the minimum free time, after the device has reached the idle state, will be as soon as the switch to low power mode. (3) Random strategy. Dynamic power management system of random switching model, and using gradient algorithm based on the vector synthetic optimal random strategy that can be used for off-line numerical calculation that also applies to the realization of the simulation method.

3. Summary and Conclusion

In this paper, we conduct research on the low power and the low voltage CMOS integrated circuit design patterns and methodologies. The improvement of CMOS process making the channel length of MOS devices appropriately smaller, which requires general lower supply voltage in chip design as the chip integration and improvement of the work clock frequency, directly lead to increase the power consumption of the chip. With the increased power consumption chip is facing the danger of high temperature work to reduce the chip and system stability. Under this condition, we propose the novel perspective on the CMOS integrated circuit design pattern that is meaningful.

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References

- [1]. Honegger, Dominik, et al. "An open source and open hardware embedded metric optical flow cmos camera for indoor and outdoor applications." Robotics and Automation (ICRA), 2013 IEEE International Conference on. IEEE, 2013.
- [2]. Salehi, Soheil, and Ronald F. DeMara. "Energy and Area Analysis of a Floating-Point Unit in 15nm CMOS Process Technology." SoutheastCon 2015. IEEE, 2015.
- [3]. Nikonov, Dmitri E., and Ian A. Young. "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking." Proceedings of the IEEE 101.12 (2013): 2498-2533.
- [4]. Yang, Fan, and Philip KT Mok. "Fast-transient asynchronous digital LDO with load regulation enhancement by soft multi-step switching and adaptive timing techniques in 65-nm CMOS." Custom Integrated Circuits Conference (CICC), 2015 IEEE. IEEE, 2015.
- [5]. Pasquazi, Alessia, et al. "Self-locked optical parametric oscillation in a CMOS compatible microring resonator: a route to robust optical frequency comb generation on a chip." Optics express 21.11 (2013): 13333-13341.