

A Design of Multi-Phase Clocks Generator for CDR

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Abstract. As a significant component of phase interpolation based clock and data recovery circuit, the multi-phase clocks generator is used to generating multi-phase clocks for data sampling. Employing the gain-boosting charge pump and the replica bias differential voltage controlled delay line for a 1.6~2.5Gbps clock and data recovery circuit, a multi-phase clocks generator was designed and implementation in 65nm CMOS standard process with 8 output clocks. Simulation results show that: the operating frequency range of the circuit is 400~625MHz; the locking time of the circuit is 400ns@625MHz; after the phase is locked, feedback phase error < 30ps, adjacent phase error < 8ps, meeting the requirements of the clock and data recovery circuit.

Introduction

Clock and data recovery circuit (CDR) is an important part of the receiver in a wired data communication system. The receiver usually streams serial data without corresponding clock. Hence, the clock must be extracted from the serial data and then resample data by extracted clock. This signal processing is called clock and data recovery [1, 2]. The CDR based on phase interpolation (PI_CDR) is a semi digital dual loop CDR structure proposed by Rambus [3]. Compared with the CDR based on PLL, PI_CDR has advantages of loop stability, short acquisition time and no jitter peaking (when loop delay time and phase update time of phase interpolator have small difference). PI_CDR could achieve 1/2 rate, 1/4 rate and even 1/8 rate structure, thus it can decrease the working frequency of the digital part of the circuit significantly, reduce power consumption and increase jitter performance. Multiphase clock generator (MPCG) is mainly used to produce the clocks with same frequency and fixed phase difference as input clock sampling high-speed serial data stream. There are two structures to achieve MPCG, one is based on PLL [5] and the other one is based on DLL [6]. Compared with the former, the latter has advantages of simple design, good stability and no jitter accumulation, which meets the requirements of PI_CDR.

The characteristic of MPCG is usually small area, fast locking and low power consumption. MPCG based on fully differential charge pump or current wheel type charge pump can improve the current matching performance of charge pump, but the structure is complicated and power consumption is too large, which is not applicable in PI-CDR. This paper proposed MPCG combination with the gain-boosting charge pump(BGCP) [7]and self bias differential voltage controlled delayed line(DVCDL), which has advantages of simple structure, low power consumption, small noise and applicable to the characteristics of low power supply voltage, to well meet the design requirements.

Background and Basic Principles of the MPCG

The basic structure of the PI_CDR. The basic structure of 1/4 rate PI-CDR is shown in Fig.1. The serial data rate is 1.6~2.5Gbps, after treatment by the analog front end equalizer (AFE), then transport into PI-CDR. The PI_CDR consist of sampler, phase detector (PD), CDR digital filter, phase interpolator (PI), MPCG and phase locked loop (PLL, not drawn in the Fig.1). The main function of MPCG is to delay and shift the clock signal generated by the phase interpolator and generate 8 stable

clocks for the sampler. In order to meet the application requirements of 1/4 data rate PI-CDR, the MPCG need to generate clocks with frequency from 400MHz to 625MHz.

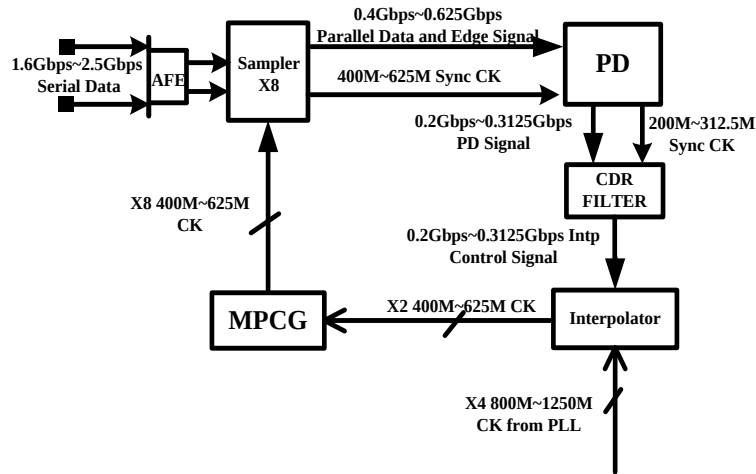


Fig.1 The basic structure of the 1/4 rate PI-CDR

Design principle and method of the MPCG. The MPCG is based on DLL. By adjusting the delay time of VCDL, the output clock Dllclk and reference clock Refclk have a consistent phase. The regulate mechanism of the DLL is Shown in Fig.2: before processing by the DLL, the Dllclk is backward to Refclk; after adjusting by the DLL, the Dllclk is pushed forward mt_d time units and eliminate the phase error between Refclk and Dllclk.

The basic structure of MPCG circuit is shown in Fig.2 (b), which is based on digital and analog hybrid DLL. The MPCG consist of Phase and Frequency Detector (PFD), GBCP, low pass filter (LPF) and DVCDL. The PFD detects phase error between Dllclk and Refclk and give results into GBCP; the output voltage of GBCP is proportional to phase error detected by PFD; after removal high harmonics by the first order LPF, obtain the control voltage of DVDCL; the DVCDL is made up with a series of delay unit with variable delay time, the control voltage V_{ctrl} is proportional to the delay time T_{VCDL} of DVCDL.

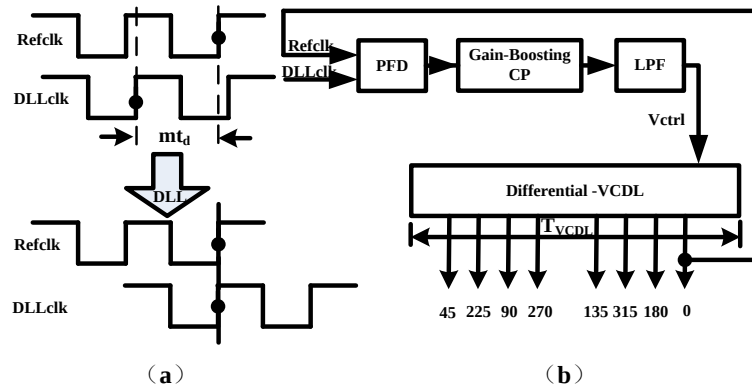


Fig.2 (a) Adjustment mechanism of DLL(b)The structure of proposed MPCG

Circuit Design of the MPCG

PFD. The D flip-flop based on the timing state models PFD is used in MPCG. There are two D flip-flop and a feedback reset logic gates in the PFD, as is shown in Fig.3 (a). The PFD and CP are usually used together, the output signals UP/DN of the PFD control positive and negative current pulse of the CP respectively, and current pulse width is proportional to the UP/DN pulse width. The input/output timing diagram of the PFD is shown in Fig.3 (b): when A signal arrives, UP signal establish immediately; then when B signal arrival, DN signal establish immediately, the Reset signal

establish subsequently and UP/DN signals are cleared to zero at the same time. A phase detect process is over.

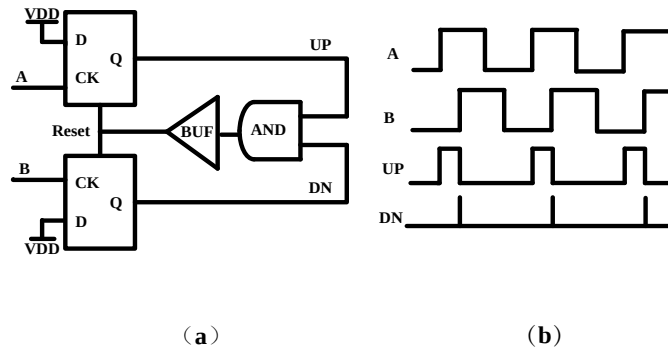


Fig.3 (a) Implementation of the PD circuit (b) Input and output timing diagram

Since limited of switch speed of CP, may the UP pulse has not to be established yet, the DN pulse has come and then clear UP/DN to zero by the Reset signal, it will cause great errors when the feedback clock and the reference clock phase error is small, so-called CP/PFD dead zone .In order to solve the problem, enough delay unit is added in Reset access, thus UP/DN signals have enough time to build up a steady current, where to eliminate dead zone in CP/PFD.

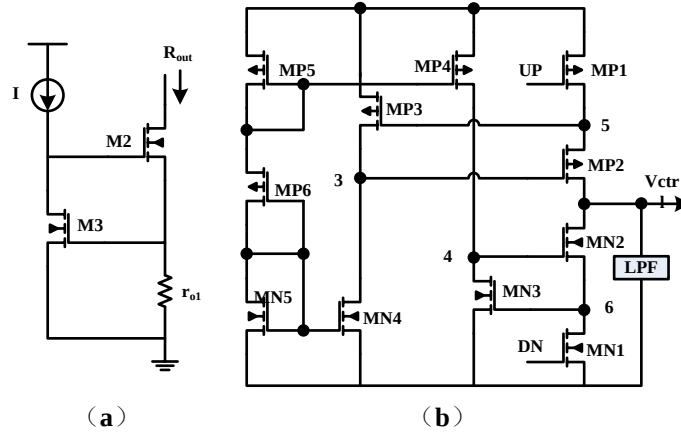


Fig.4 (a) Gain-boosting circuit (b) Implementation of the gain-boosting CP

GBCP. It is a big problem plagued CP caused by the charge sharing effect, so-called current mismatching. Through increase the equivalent output impedance of the current source, it can effectively suppress the charge sharing effect. An effective ways to increase the equivalent output impedance is using the structure of Gain-boosting, as shown in Fig.4 (a), the equivalent output impedance is:

$$R_o = g_{m3}r_{o3}g_{m2}r_{o2}r_{o1} \quad (1)$$

The Implementation of the GBCP of transistor level is shown in Fig.4 (b). The left part constitute of MP4, MP5, MP6,MN4 and MN5 is the current mirror circuit, provides bias voltage for MP2 and MN2, so that they will work in the linear region; the right part is the optimization of the gain-boosting circuit, including MP1, MP2,MN1 and MN2. The Fig.4 (b) also gives LPF model and a capacitor can be used to achieve it.

DVCDL. The DVCDL is mainly composed of 6 differential delay buffer (DB) [8] and a replica bias circuit (RBC) [9]. The DB is mainly composed of a symmetrical load, a pair of NOMS switch and a dynamic bias NMOS current source, as is shown in Fig.5 (a). The DB has good noise suppression ability as following reasons: first, under different control voltages (V_{ctrl}), the symmetric load has a center symmetric I-V characteristic curve between the V_{ctrl} and the supply voltage VDD, its equivalent load has a high degree of linearity, can be dynamic offset noise coupling, to obtain a good ability to suppress the power supply noise; second, the differential structure can suppress the common

mode noise introduced by the environment or VDD; third, RBC provides a bias voltage independent of VDD and substrate voltage for the dynamic bias NMOS current source, thereby providing pure bias current for DB; At the same time, the feedback structure formed by RBC and DB, can dynamic adjust the size of tail current source by Vctrl, equivalent to increase the output impedance, thus obtaining a similar inhibition of substrate noise with cascade current source structure

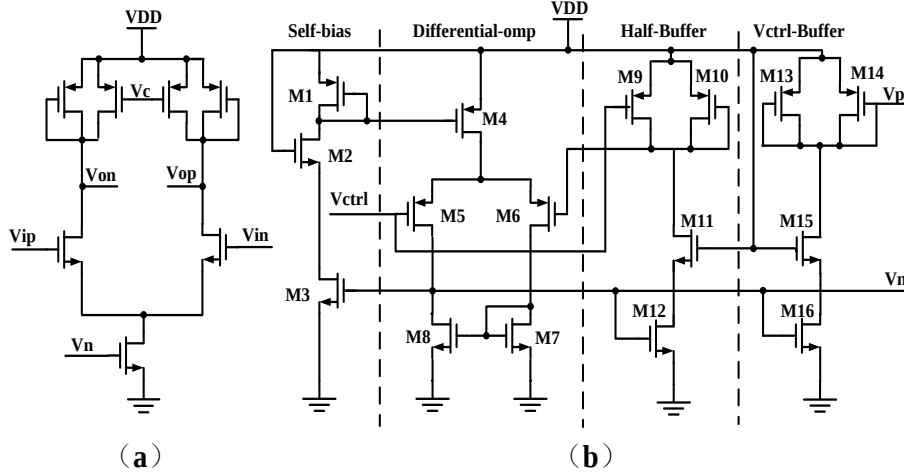


Fig.5 (a) Delay element with symmetric load (b) Replica bias generating circuit

RBC is shown in Fig.5 (b). The circuit is mainly composed of self-bias stage, differential-omp stage, half-buffer stage and Vctrl-buffer stage. The main function of the circuit is to generate bias voltage of dynamic bias NMOS current source Vn and the symmetrical load bias voltage Vp. With the same bandwidth of RBC and DB, so as to be able to track the different frequency of the adjustment; The differential amplifier feedback regulation of Vn, makes Vp equal to Vctrl; another reason for using the Vctrl-buffer stage is that the stage is able to isolate the potential capacitive coupling between the Vctrl and DB, thereby obtaining better circuit performance.

Simulation Results

The definition of current matching characteristics is [7] :

$$\frac{I_{UP} - I_{DN}}{I_{UP}} = \frac{\Delta I}{I_{CP}} = \frac{\Delta V}{I_{CP} \cdot R_o} \quad (2)$$

The MPCG is simulated by spectre with 65nm 1.2-V CMOS process. The GBCP current matching characteristics simulation results are shown in Fig.6. By the figure, in discharge process, the range of Vctrl is 1.105~0.3911V and discharge current is stable at about – 488uA, Range of change less than 0.3%; in charge process, the range of Vctrl is 0.070~0.710mV, the charging current is stable at about 488uA, Range of change less than 0.2%. According to formula (2), current matching characteristics less than 0.7%, the matching degree of current is small, to meet requirements of the design. The effective range of Vctrl is 0.3911~0.710V.

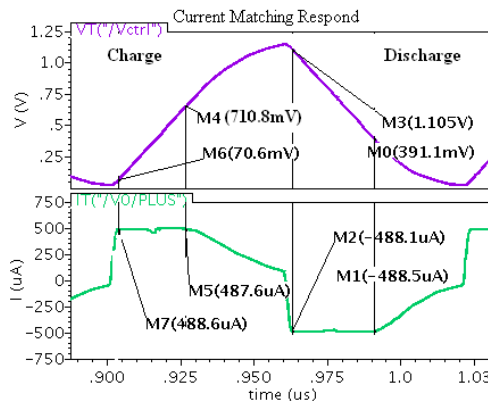


Fig.6 The results of Charge/discharge current matching

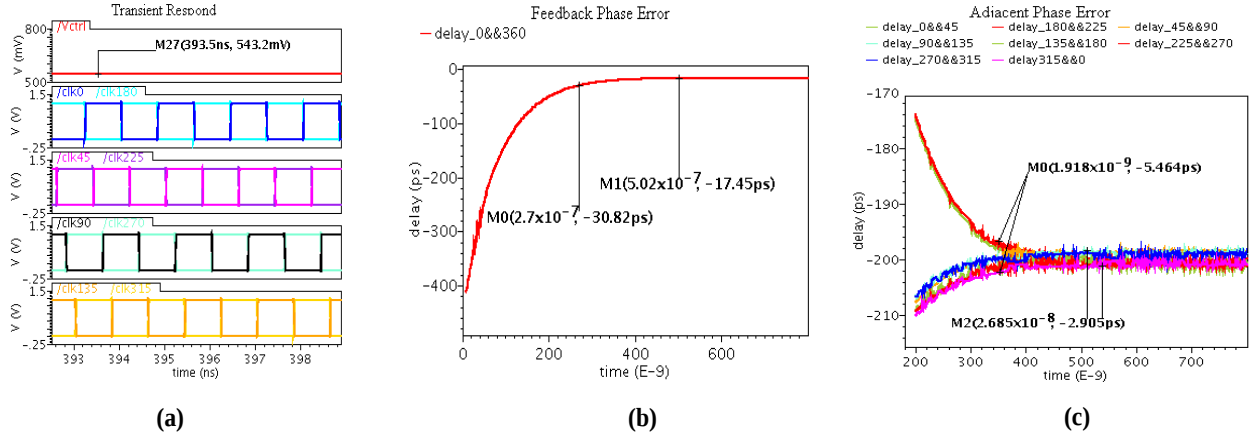


Fig.7 (a) Transient Response (b) Feedback Phase Error (c) Adjacent Phase Error

The overall simulation results of MPCG are shown in Fig.7. Among them, Fig.7 (a) is the transient simulation results at 625MHz (@TT); Fig.7 (b) is the simulation results of feedback phase error; and Fig.7 (c) is the simulation results of adjacent phase error. It can be seen from Fig.7 that the phase locking time is about 400ns; after locking, the charge pump control voltage is about 543.3mV, the feedback phase error is about 17.45ps, and adjacent phase error is about 3ps.

Tab.1 Simulation result of feedback & adjacent phase error

Frequency	Feedback Phase Error	Adjacent Phase Error
400MHz	18.33ps@tt	2.58ps@tt
	20.78ps@ss	6ps@ss
	26.4ps@ff	7ps@ff
	17.45ps@tt	3ps@tt
625MHz	20.33ps@ss	5ps@ss
	25.35ps@ff	6ps@ff

Tab.1 presents the simulation results of the feedback phase error and adjacent phase error in different technological corners. It can be seen from the table, the feedback phase error in the 650MHz@SS is worst, but no more than 30ps; the adjacent phase error is less than 8ps in all corners, to meet application requirements of PI-CDR.

Conclusions

Employing the gain-boosting charge pump and the replica bias differential voltage controlled delay line, a MPCG for PI_CDR is proposed. It can produce 8 sampling clocks with stable frequency and phase difference is $1/4\pi$. The structure is simple and does not require an additional band gap voltage source to provide bias. The ratio of the loop bandwidth to the fixed frequency follows the variation of the operating frequency. Compared with MPCG based on PLL, it has shorter locking time, to meet requirement of PI_CDR.

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