Design of Single - photon pulse generator based on FPGA

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Abstract. Based on the PMT test system analysis, from the perspective of PMT single photo-electron peak starting to get accurate test existing test pulse generator is optimized to achieve the interactive system and PC control system through the ARM controller, through the FPGA to achieve adjustable duty cycle pulse width output, to achieve the output datum transformation through the level conversion chip and programmable voltage source, and ultimately the high-precision, multi-channel pulse generator, and the output signal quality pulse signal generator and RIGOO-DG5352 350MHz analog output signal source for comparison, the rise time, fall on superior signal source parameters currently used time. And expand the design is better, you can compare the signal source quickly expanded into more channels compared to conventional sources, only 2 channels or 4 channels more suitable PMT test system.

Introduction

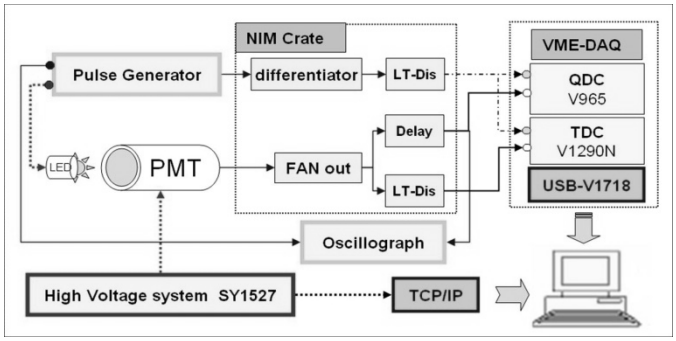


Fig.1 Electronic schematic of PMT test system

In recent decades, with the development of technology, many large particle physics experiment using photomultiplier PMT for photon detection and record. Sophisticated pulse signal is usually used to be the testing and calibration for PMT. Generally commercial pulse generator, such as

RIGOO DG5352 analog bandwidth of 350 MHz ,but only has two channels. Similar the channel of the commercial pulse generator is usually 2 or 4, which cannot satisfy the physical experiment. Setting up such a test platform is very complex and cost with commercial pulse generator. The project is to design a kind of multi-channel pulse signal generator based on Ethernet, highest number can reach 32 channel s, and can be applied on a large PMT system of testing and calibration.

During the experiment, in order to know the time performance of PMT and absolute Gain (Gain), the energy resolution (σ),along with the change of high voltage (HV) ,VME test system as the core to set the PMT.Thetest device used: pulse generator drive diode (LED), driving frequency of 1 KHZ, illuminates the PMT photo-cathode and by anode output as QDC testing signal, at the same time the pulse synchronization output through a differential circuit into low threshold discriminator (LT - Dis) output as the testing signals of open the door signals .

In this design , the pulse generator signal is used to drive the LED, characteristics of pulse generator about time and amplitude characteristic will have larger influence on luminescence characteristics of LED,and it will affect the test accuracy of PMT. For this system, the parameters of the pulse generator in relatively care about are: rise time, fall time, frequency, duty cycle, output electricity equal and so on .According to the requirement of the PMT time testing system, this design designed a set of PMT photo-cathode test LED driver source system.

Hardware Design

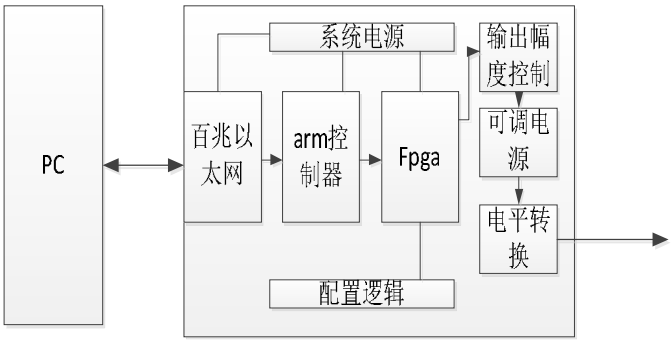


Fig. 2 Hardware Design

In this system, FPGA cooperate with adjustable phase locked loop for outputting the pulse frequency of clock, controlling duty ratio,output voltage level and signal output module to achieve transformation of output level,output amplitude, and to enhance the output driver and so on.The module of output amplitude controlledadjust the output level; The arm controller and 100M Ethernet chip are connected with PC to parse PC command and controlthe system. FPGA using Altera max10 series is the latest FPGA of Altera . This series of FPGA of the28nm processhave the characteristics of high working frequency,low power consumption and so on. As the core of the system.

FPGA is responsible for the generation and the control of the pulse signal.ARM controller using the stm32f107 of st company,cortex-m3 as the core, with the highest working frequency for 72MHz,with very rich peripheral interfaces ,can connect with 100M Ethernet physical layer chip by physical mii/gmii interface layer. Dp83848 is Ethernet physical layer driver chip for TI company, which support 10 m / 100 m adaptive and connect to MCU through the GMII/MII interface .The

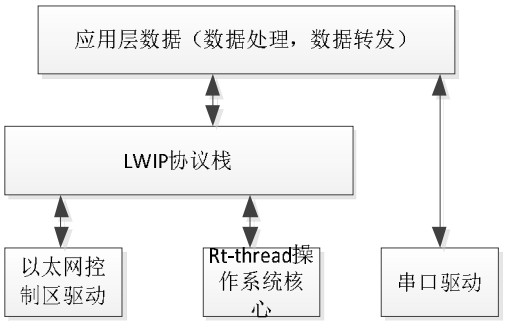
level converter chip as the controllerofoutput to change the signal level without causing the signal distortion .This level conversion chip supports the maximum digital frequency is above 500M. The output voltage of the chip is provided by the programmable precision voltage source,which is composed by adjustable resistorandlow-dropout regulator.The output voltage of the low-dropout regulatoris determined by the feedback resistor. The formula is 1.2*R1/ (R1+R2);Controlled by FPGA, can change the value of the adjustable resistor, the value of the R1 and R2 that access to feedback circuit , eventually can form the adjustable voltage source, the capacity of voltage source output is 200MA, which can drive two way level conversion chip.The resistor is a1obit high resolution adjustable resistor, by using this the voltage resolutionof the output level is 3.6/(2^10). The resistance error is 1%and the value range is 0~ 20K ,So the output voltage range is 1.2V~3.6V.

The whole working process of the system is: After receiving the command from the PCthrough the Ethernet, the MCU receives the data and forwards it through the Ethernet. Thereceived data contain the following information: level range, duty ratio and cycle.The data is calculated in the MCU and transformed into the following parameters :the value of source voltage feedback resistor resistance R1, R2 with 16bit , high level time T1 and low level time T2 with 4bytes,all the data is 12 bytes.Every time before sending data, MCU will synchronouslymake IO pin low as written data frame identification .when IO for low said start of data frame, while the high said end of the data frame. FPGA will analyze the data frame, then send the R1, R2, T1, T2 to the corresponding registers. At the same time, it will start the forwarding part of the logic ,write the value of R1, R2 to the adjustable adjustable resistorthrough the SPI interface ,and write the value of T1, T2 into FPGA internal register.

Software Program Design

Software program contains three parts: PC software, embedded applications and the FPGA logic.

Embedded Program Design.



Embedded program mainly is the part of the control program about ARM controller STM32F107 , this part of the program is mainly implements the TCP/IP protocol stack, through TCP/IP protocol to receive Ethernet datasentfrom the PC . And in the application layer to deal with and transmit the data . The embedded code structure as follows:

Fig. 3 embedded program design

Achieved the Ethernet chip driver of transplantation and application layer program based on the rt-thread within the framework of the operating system. The main data flow for MCU program code as follows: Firstly,testing the package integrity after the data through Ethernet input,then,converting data about duty ratio of the input,leaveshift and etc. The data will be converted into the FPGA corresponding register values . The corresponding register includes: 1 high level time. 2 low level time. 3 adjustable resistance.4 Delay between channel. Through the USART interfaces, the CPU writes values into the corresponding register to achieve control of the FPGA**.**

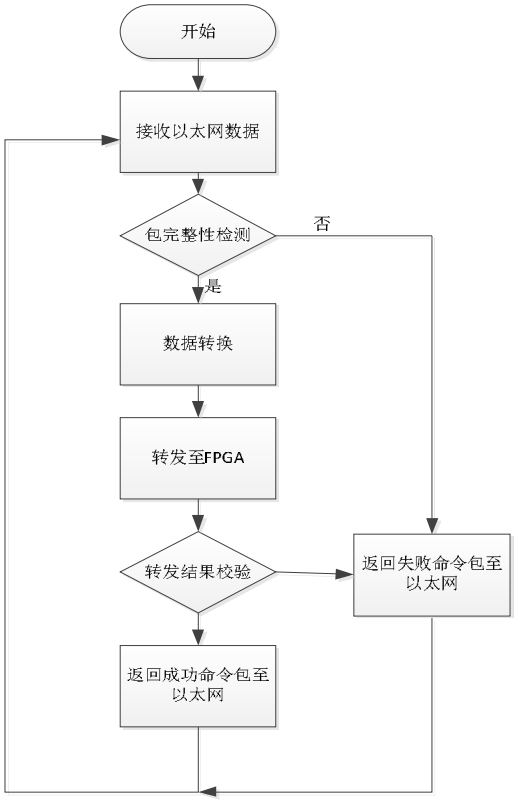


Fig. 4 Program Design

FPGA Logic Design

The FPGA logic mainly includes distribution and reception of data,etc.FPGA receive the data value sended from thre mcu by usart,and then check its integrity, finally write to register. The high level and low level time register deal with data in the fpga , then adiust the phase of the fpga internal phase-locked loop output clock . The different phase of the pulse signal with the AND logic output producing a waveform. The values of adjustable resistor register, through the SPI interface into to the adjustable resistance,which is used to control the voltage of the feedback about low-dropout regulato, and then control the output of low level. The values in the channel delay register are sent to the counter to control the time delay between the channel. Finally configuration about cycle of each channel signal, duty ratio, the channel delay, output level will be completed in FPGA.

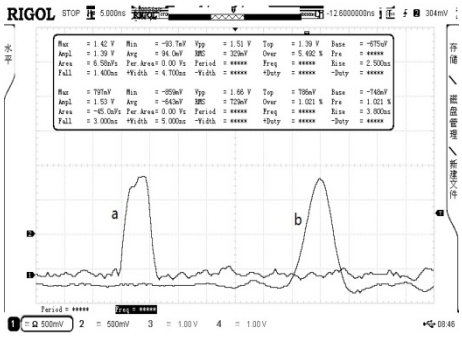
After compare test, found that the posedge is about 1.3 ns, negedge is about 1.5 ns, the shortest level lasts 5 ns, adjustable voltage range of 1.2 V to 3.3 V, drive ability of one way is about 40 ma single way.

Test results

The follow picture is about the system with RIGOO DG5352 signal source output waveform for comparison, RIGOO DG5352 is the RIGOO company's signal source, maximum output analog bandwidth is 350 MHZ, the output sampling rate is 1 GSPS, blue wave (oscilloscope channel 2)is signal source output waveform. yellow waveform (oscilloscope channel 1 is the system output waveform). Test using oscilloscope model for RIGOO DS6104 oscilloscope, the bandwidth of the oscilloscope is 1 G, sampling rate is 5 GSPS, cooperate to use 1.5 G analog bandwidth probe.

From test results can see the output waveform characteristics is:

	DG5352output	Test systerm output
Rising edge	3.800ns	2.500ns
falling edge	3.000ns	1.400ns
frequency	1~350MHz adjustable	0.01Hz~300 Mhz adjustable
duty ratio	adjustable	adjustable
Singal leavel	0-10V adjustable	1.2 ～ 3.6V adjustable



Through the contrast can be seen signals overshoot, rise time, fall time is superior to RIGOO signal source**.**

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