

Study of Failure Analysis of Power Transistors

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Abstract. This paper present a process of failure analysis which, to some extent, can demonstrate a variety of failure process in regard to power transistors. General failure analysis process will be introduced at the beginning of this article. The test objects are power transistors which were found to be the fundamental cause towards failure of control system. Specifics of test procedure will be disclosed as below in the text. The procedure of failure analysis was conducted through comparison. Through integrating examination, inspection result and deduction, outcome illustrates that the interaction of congenital defects and ambient activation in use contribute to failure. Ultimately, given the inferences that inherent defects existed before employment, and that adverse ambience aggravate the damage of components, we will propose conclusion and opinions on production. The possibility that failure analysis makes power transistors more reliability will sustain our endeavor.

Introduction

Power Transistor. Low frequency power transistors are employed in the circuit of low frequency amplifier, voltage regulator and oscillation. High voltage power transistors are applied to the circuit of scanning, oscilloscope deflection, radar display and high voltage switch which are a vital component of television. To some extent, power transistors, combined with technology and imagination, built electronic equipment.

Generally, a transistor whose power dissipation is more than one watt can be stated as a power transistor. Apparently, it conceives a constitutional property—it, compared with others, has greater power dissipation. According to the case of failure analysis(FA) from five centers of failure analysis, it was proposed that almost 90 percent of failure was due to over current or voltage and thermal failure originally resulted from its greater power.[1] This is the very reason why the reliability and life-span of power transistor still stay in unsatisfactory performance even if experts and scholars paid close attention. Sankin, I applied a new monolithic SiC NET IC technology for high-temperature smart power applications that allows for on-chip integration of control circuitry and normally-off power switch which had a limited effect on dissipation of power transistors.[2] In perspective of simulation, H. V. Nguyen deemed that electromigration simulations using a two-dimensional simulator confirm the extrusion short circuit as failure mechanism.[3] Thomas D. Moore examined common modes of structural failure through stress simulation.[4] However, they both concentrated on simulation aspects. In fact, FA emphasize analysis of specific experiments.

Failure Analysis. Science is always linked with creation. However, damage is also a science. Failure analysis is a science of damage. To be specific, some sections in FA are destructive so that components after this are destroyed. Destruction is the means, but creation is the goal.

Failure analysis is a probing method between knowledge and skills. In one respect, FA is an ability that has been acquired by training which can be regarded as skill, and only practice makes it perfect. On the other side, FA must combine with knowledge—the psychological result of perception and learning and reasoning which means it is an ephemeral process of comprehension. The correlative knowledge concerned with background and component can lead us to the answer. FA on power transistors conducted in the paper demonstrate inferences and issues in the way of ab uno disce omnes.

The article does not involve software simulation and modeling, but focus on experiment operations and results analysis. Actually, FA is only related to specific operations and theory deduction from failure physics.

In this paper, FA be conducted with case analysis of power transistors. Finally, conclusions of failure process and opinions on production will be brought forward.

Case Analysis of Power Transistors

Test Objects and Principles. Several power transistors are objects for study of FA. Power transistors of the same lot which are organized as comparison#1, #2and #3 are compared with the failure during case analysis.

The principle and process of FA are circumstantial except that the nondestructive steps should be conducted before the destructive ones. It is why external inspection and electrical performance test are implemented before internal inspection which is destructive. Actually, X-ray inspection, examination of optical microscope and ingredient analysis are carried out based on certain circumstance which means they aren't inevitable segment of FA.

Case Analysis. Universally, external inspection (Fig. 1) is the first step of FA.



Fig. 1 Appearances of failure (L) and comparisons(R)

It turns out that the failure almost show no difference from comparisons through the examination of optical microscope. However, electrical performance test (Tab. 1) at ordinary temperature proves that electrical properties of the failure are completely disordered. It's obvious that the failure is bad performed because parameters of BVCEO (opposite breakdown voltage between collector and emitter) and HFE (a criterion for Static current amplification factor) are disordered.

Table 1 electrical performance test

Parameters	BVCEO(V) VCEmax=120V ICE=5mA Min=100V	BVEBO(V) VEBmax=10V IEB=20mA Min=5V	HFE(V) IC=10A VCE=10V Min=500V	VCESAT(V) IC=10A IB=200mA Max=3V
Comparison1#	210.0	10.00	6640.8	0.952
Failure	0.248	10.00	0.0	1.010

In order to investigate disordered properties, internal inspection(Fig. 2) were implemented and it disclosed several weaknesses and flaws. There are two distinct cracks penetrating chip and a mark of burnout and solder leakage which are absent in comparisons.

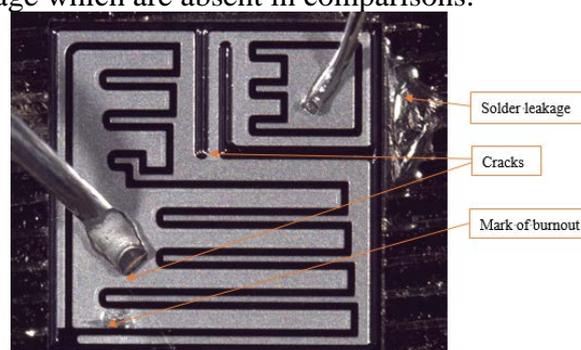


Fig. 2 Internal inspection

Two distinct cracks penetrating chip(Fig. 3): to some extent, they are the most intuitionistic state we learned which could directly lead to failure;



Fig. 3 Cracks in detail

Mark of burnout: it results from localised overcurrent damage. In some respect, fatal cracks localise the mark of burnout. However, the most fundamental reason due to burnout could be welding hole inside the chip;

Solder leakage: solder below a side of the chip overflows which is consistent to principles for rejection of GJB-128A——Test methods for semiconductor discrete devices.[5]

Generally, localized overcurrent damage bring chain reaction, and it is accompanied by other flaws like welding hole

In order to probe into the assumption which is localized overcurrent damage could contribute to the existence of welding hole inside the chip, X-ray inspection is a feasible way to research. However, both the failure and comparisons turned out no welding hole. Hence, this speculation was overturned.

Examination of optical microscope led to another clue. Concretely, we checked the quality of welder layer after chips were removed. Large tan interface were found from solder layer of all chips except comparison 1#. The region of tan interface of comparison 3#(Fig. 4) exceeds 60 percent of welding area of chip. In addition, the region of tan interface of both the failure(Fig. 5) and comparison 2#(Fig. 6) approximately occupy 20 percent. We should take this possibility into consideration that it comes out failure of batch.



Fig. 4 Tan interface on solder layer of the failure

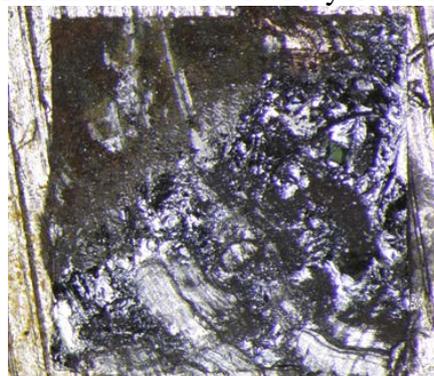


Fig. 5 Tan interface on solder layer of comparison 2#

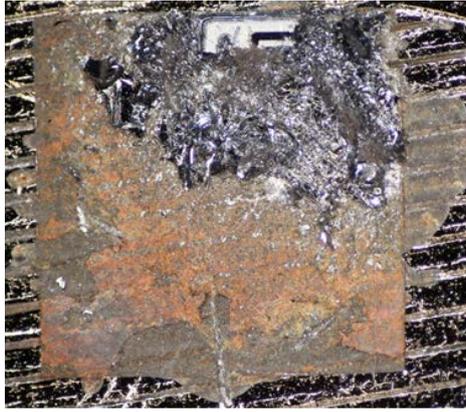


Fig. 6 Tan interface on solder layer of comparison 3#

In order to clarify the ingredient of tan interface, examination of electron microscope was conducted in this section. According to the instruction of manufacturer, ingredients of solder layer are mainly compound metal of Pb-In-Ag of which content of Pb dominate 92.5 percent. However, detection result revealed that elements of carbon and, especially numerous content of oxygen existed. Region of examination and situation of ingredients analysis are shown in Fig 7 and Fig 8. Concrete numerical value of element are as follows(Tab. 2).

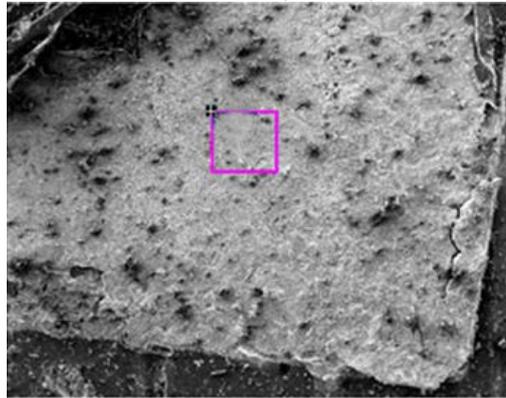


Fig. 7 Examination of electronic microscope

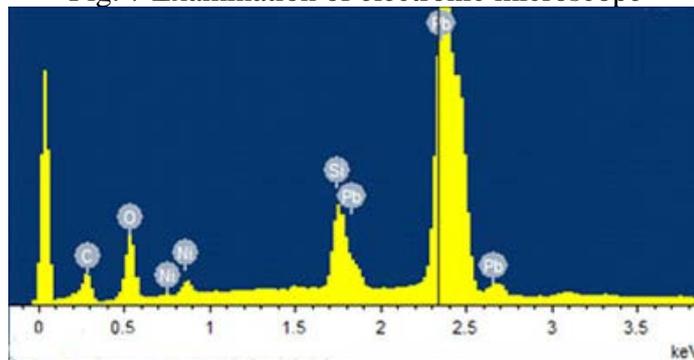


Fig. 8 Ingredients analysis of pink region

Table 2 numerical value of element

Element	Weight percent	Atomic percent
C K	7.73	31.55
O K	13.92	42.66
Si K	4.61	8.05
Ni K	0.47	0.39
Pb M	73.28	17.35
Gross	100	100

Analysis and Summary The fact we cannot deny is airtightness of components was compromised before they came into service because both failure and comparisons were found with tan interface which was oxidized. Because result of ingredients analysis displayed the existence of

oxygen which shouldn't be involved. To testify this, other transistors were brought to seal test. This proved the very inference.

There are several doubts about data shown in Tab 2. Where were C, Si and Ni from? And where did In and Ag (ingredients of solder layer) go? Actually, the surface we test and analyzed is between chip and solder layer. This's why chips were removed before we checked the quality of welder layer. Where were C, Si and Ni from? They came from chip. C, Si and Ni are common materials for chip. Material bonding because of high temperature working condition left trace of such elements, especially C and Si. Ingredients analysis was conducted by electronic energy spectrum analysis instrument. This instrument of UV-light acting the role of the excitation sources only act on the sample surface, and obtain the distribution of information of photoelectron energy finally. It is the reason why In and Ag were not displayed in the outcome. Electronic energy spectrum analysis instrument only analyzed the surface. Spectroscopy of Ag and In are similar, not to mention the situation that their element content is extremely rare. These with the addition of the fact that solder layer surface attached residual material of chip contribute to the disappearance of Ag and In. removing the surface, we'll find their existence.

Backtracking the entire experimental process, we can conclude that inherent defects existed before components came to employment. Tan interface is the best proof. However, what confuse me is that these components possessing flaws pass the qualified test. But, if we observe these interface carefully, such detail won't be miss that tan surface of the failure showed different from it of comparison. Color of the failure looks like something burnt but hue of comparison performed something gentle. So, it could explain why comparisons' electrical performance test passed.

Although components having such defects wouldn't be granted in standard, flaws have little or no influence on properties. In other words, sometimes inherent flaws in component is harmless in early application, but their harmfulness will gradually reveal. Electronic properties seemed immune to congenital flaws, but thermal dissipation is strongly affected by oxide layer. Localized overcurrent resulted from poor heat dissipation is the most reasonable explanation for burnout. Solder leakage could be brought from this. As for cracks which are the fatal and intuitionistic account for failure, congenital defects and ambient factor contributed to malfunction. So, environment activate these inherent defects. Burnout, solder leakage and cracks are the performance and outcome of activation.

Conclusion

FA demonstrate the conclusion concerned with failure cause that the interaction of congenital defects and ambient activation in use brings failure. To be exact, such constitutional defects as above owing to problems in production are the first step toward failure. Airtightness of components was compromised and solder layer was oxidized before they came into application. These flaws are activated by hostile ambience. Complex environment stress condition during usage aggravate the damage of components It's the second step. Finally, local overheating creates thermal stress which leads to chip cracking. The combination of connate defects and adverse ambience causes failure.

Failure was not built on an accident just like Rome was not built in a day. This failure is of batch. The production process need to be inspected and supervised, especially the package stage. Manufacturer should take seal test in their qualified test or improve packaging technology.

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