Development and Verification of A Small CMOS Digital Standard Cell Library Based on SMIC 130nm Process

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Abstract. Nowadays, Semi-custom design based on the standard cells is the mainstream design method for digital IC chip. In this thesis, the standard cell library is built and verified based on the SMIC 130nm technology, especially the optimization of a 1-bit full adder cell, during which the structure and layout of the full adder in the SMIC library is analyzed. As a result, the structure and size of the adder cell are improved better, which is simulated by H-spice. The comparison shows that the optimized adder is not only smaller in area, with width decreased by 0.82μm, but also have advantages in power consumption and timing, with energy delay product reduced by 7.7% .In the end, the s298 circuit in ISCAS Benchmark89 is used as the benchmark to complete the verification method of the standard cell library.

Introduction

Standard cell library is the basis of gate-level module based circuit design, and it has a direct impact on the performance[1,2], power consumption, size and yield of the final flowing out circuits. Since the standard cell library has an important position in gate-level module based circuit design and the requirements of standard cells' performance[3], standard cell itself is done through the full custom design. A library unit is infinitely rich in theory, the more the better. From this point of view, it will take a long time to complete the full custom design of standard cells. Building the standard cell library needs to do a lot of work[4], and requires a significant investment of human and financial resources. By optimizing the structure and layout of the standard unit, the properties of the standard cells which we get perform more excellent than the standard cells in the SMIC13 library.

Standard Cell Library and the Process of Standard Cell Library

The Composition of the Standard Cell Library. Standard cell library includes many libraries such as map library, symbol library, sequence libraries, physical library, simulation library, etc. Layout library is the subject, which will be invoked by EDA tools in the back-end process of IC design to generate the actual physical layout of the chip. Physical library is the abstract description of layout library, keeping only the physical port information in order to easily route and optimize for EDA tools[5]. Symbol library is a visual description for identifying, which provides symbols when displaying circuit schematic. Timing library is extracted when the standard cell is characterized. It contains the timing information used by EDA software in static timing analysis, logic synthesis and optimization. Simulation library is the Verilog or Vhdl description file of the cell library, used in former simulation and after simulation in IC design. Synthesis library is used to extract characteristic parameters of all the logical units of functionality[6], and get comprehensive information such as timing, power, and logic function in the lib format of model data.

The Process of Standard Cell Library. The following Fig.1 is the process of standard cell library building.
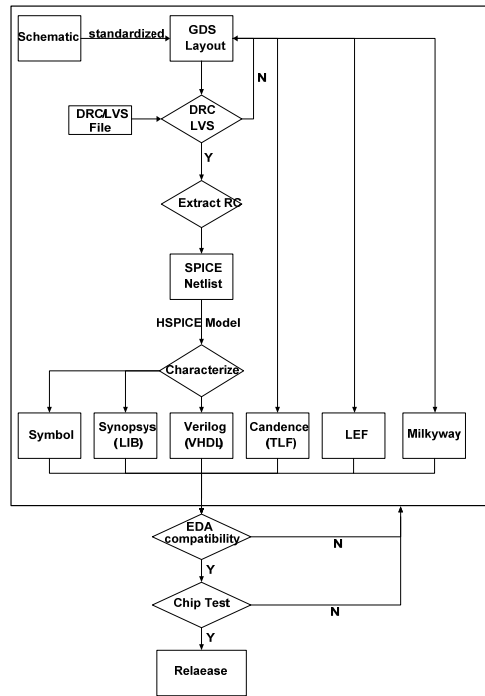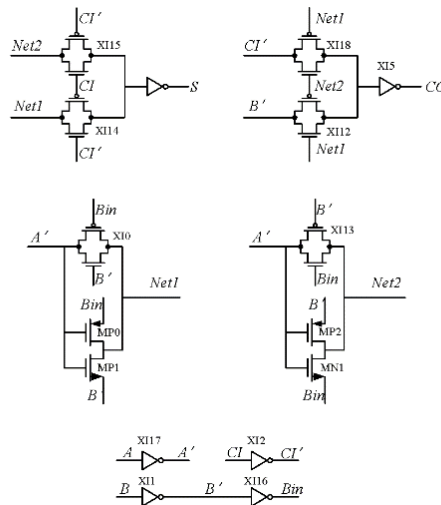
Figure 1. The process of standard cell library building

The Optimization of the 1-bit Full Adder Cell

Structure and layout of the full adder in the SMIC library and the optimized full adder cell are shown in the follow Figures.

Figure 2. Structure of the full adder in the SMIC library

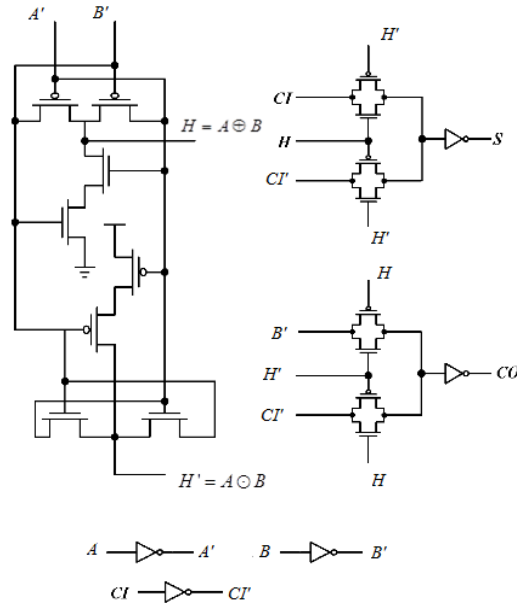Figure 3. Layout of the full adder in the SMIC library
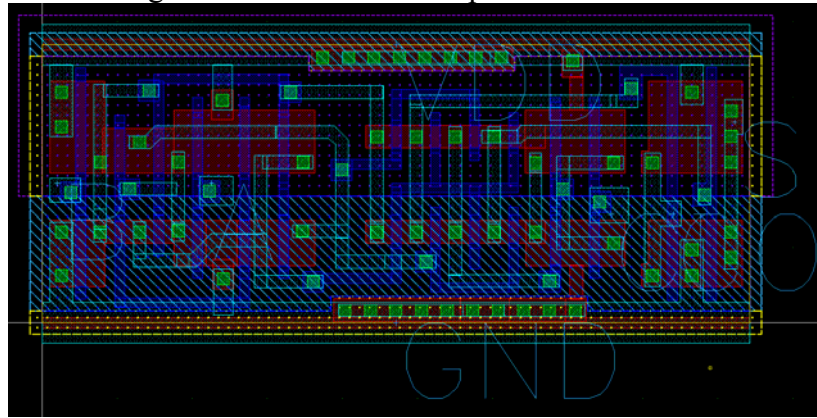
Figure 4. Structure of the optimized full adder

Figure 5. Layout of the optimized full adder

The inverse relationship between signal A and A', B and B', CI and CI', H and H' are shown in the Figure 2 and Figure 4.

By ordering $H = A \oplus B$, $H' = A \odot B$, it is obviously to see that the H and H' circuit are the most difference between the two full adder cells. Standard cell library contains CMOS inverters and CMOS transmission gates while we use PMOS (NMOS) transmission gates and pull down MOS transistors in series to get H (H') in the optimized cell. When the signal A and B are in at least one high level, the two PMOS transistors will have at least one conducts. Thus the Boolean expression is $AB' + A'B$. On the other hand, when A and B are both low, the two PMOS transmission gates are closed. According to the function, output should be in low level, so we use two pull down NMOS transistors in series, whose gates are connected to A' and B', then the conducting state guarantee the function is right. By combining two parts, we can get the Boolean expression $H = A'B + AB' = A \oplus B$. When signal A and signal B are in at least one low level, two NMOS transmission gate are in at least one low level, then the Boolean expression is $A'B'$. when signal A and signal B are both high, two PMOS conduct and pull H' up to the high level, the Boolean expression is AB. Combining the two parts, we can get the Boolean expression $H' = A'B' + AB = A \odot B$.

Results

FA_1 is the full adder in the SMIC library and FA_2 is the optimized full adder, the comparative results are measured as follows:

Input Pin Capacitance. Because of the smaller transistors, three input capacitances in the optimized full adder are smaller than the original cell. The comparison is shown in the Table 1.

Table 1. Input pin capacitance

Full Adder	Pin		
	A (fF)	*B (fF)*	*CI (fF)*
FA_1	6.41	4.98	4.94
FA_2	2.91	4.02	3.03

Static Power Consumption. After optimized the full Adder has smaller size, and the static power consumption is reduced by 15.6%. The comparisons are shown in the Table 2.

Table 2. Static Power Consumption

Full Adder	ABCI(nW)								average (nW)
	000	*001*	*010*	*011*	*100*	*101*	*110*	*111*	
FA_1	21.7	24.1	24.2	19.5	24.2	24.9	25.0	22.0	23.2
FA_2	14.7	19.0	22.4	19.7	19.5	22.1	20.2	18.9	19.6

Propagation Delay. By using the smaller transistors, the timing performance of the optimized full adder is weaker than the original cell. The propagation delay has increased by 0.79%. The comparison is shown in the Table 3.

Table 3. Propagation Delay

Full Adder	Propagation delay(ps)						average (ps)
	1	*2*	*3*	*4*	*5*	*6*	
FA_1	144.8	126.0	138.4	135.7	132.9	126.2	134.0
FA_2	141.7	138.8	137.4	133.8	128.5	130.0	135.0

Dynamic Power. Because of the smaller size, the dynamic power of optimized full adder is reduced by 8.49%, the expected results have been achieved. The comparison is shown in the Table 4.

Table 4. Dynamic Power

Full Adder	Dynamic power(μW)						average (μW)
	1	*2*	*3*	*4*	*5*	*6*	
FA_1	48.25	45.95	48.96	47.68	40.90	43.70	45.91
FA_2	43.01	42.56	41.52	42.93	40.06	41.99	42.01

Energy Delay Product. EDP (Energy Delay Product), is a widely used method for measuring cell speed and delay. In order to measure the performance of two full Adders, EDP is used as indicators. The comparison are shown in the Table 5.

Table 5. Energy Delay Product

Full Adder	switch energy (fJ)	Propagetion delay(ps)	EDP(pJ·ps)
FA_1	63.76	133.98	8.54
FA_2	58.35	135.04	7.88

From the table, thanks to the good circuit with optimized architecture as well as the reduced circuit size, optimized full adder in EDP indicators has reduced by 7.73%.

In summary, the optimized full adder has decreased width by 2Pitch and size by 8%; slightly weaker in timing, delay increases by0.79%; 8.49% lower on dynamic power consumption, static power consumption has reduced by15.6%; EDP has reduced by 7.73%.

The Verification of the Standard Cell Library.

The small scale circuit s298.v belongs to Benchmark89, which is chosen from official website of ISCAS, it contains 14 D-type flip-flops, 44 inverters , 75 gates(31 ANDs +9 NANDs+16 ORs +19 NORs); in total of 133 instances, which can be used to go through the total process of the digital IC design to get the layout. The Figure 6.
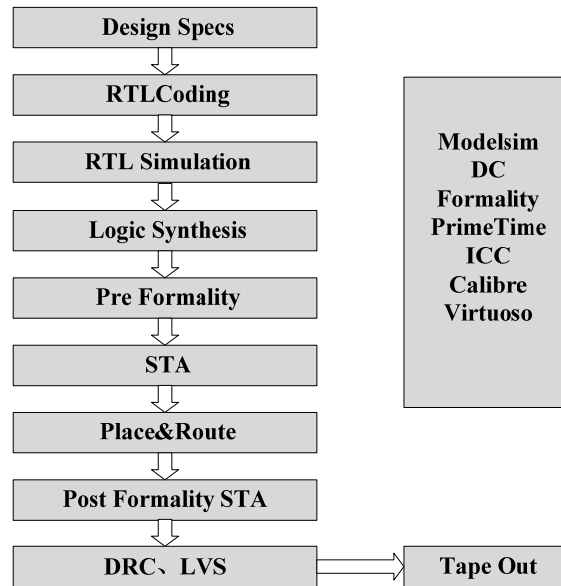
Figure 6. The total process of digital IC design

Layout Verification

According to the description from the official website, Benchmark89 s298 which we use is a program for the control of traffic lights:

Remove clock CK, there are three inputs (G0, G1, G2) and six outputs (G117, G132, G66, G118, G133, G67). G0 is a reset signal, active high and synchronous reset. G1 is the input control modes. G2 is the input to control the flash of the lights.

Green: G67/G66

Red light: G118/G117

Yellow light: G133/G13

The simulation results are obtained under the control of various modes, as the following show:

G1=0, G2=0: 1th light: the simulation waveform as shown in Figure 7. The figure shows that there are 14 cycles of green G67, 2 cycles of yellow G133, and 4 cycles of red G118.

2nd light: the simulation waveform as shown in Fig.8. The figure shows that there are 2 cycles of green G66, 2 cycles of yellow G132, and 16 cycles of red G177.
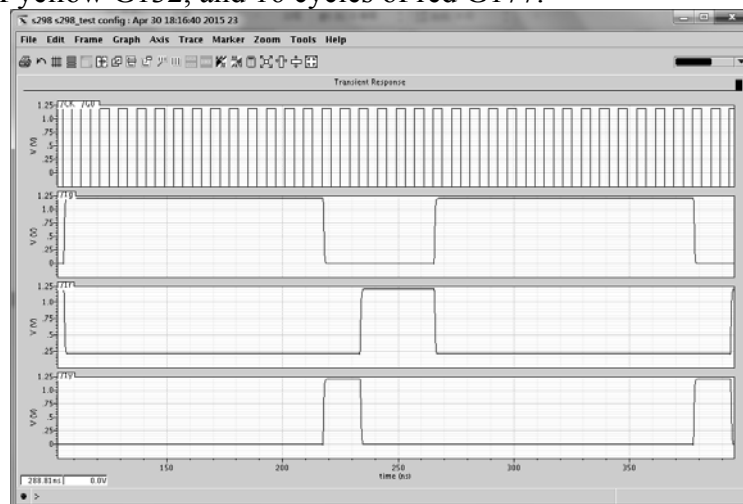

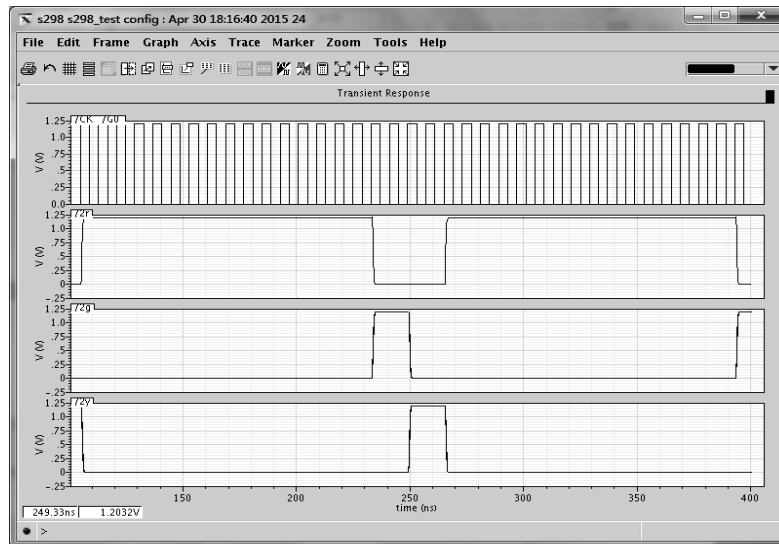Figure 7. G2G1(00) the post-simulation waveform of 1th light

Figure 8. G2G1(00) the post-simulation waveform of 2th light

G1=1; G2=0: 1th light: The post simulation waveform as shown in Figure.9. The figure shows that there are 8 cycles of green, 4 cycles of red, 4 cycles of yellow, and 4 green.

2nd light: The post-simulation waveform as shown in Figure 10. 8 2 red 2green yellow 8 red
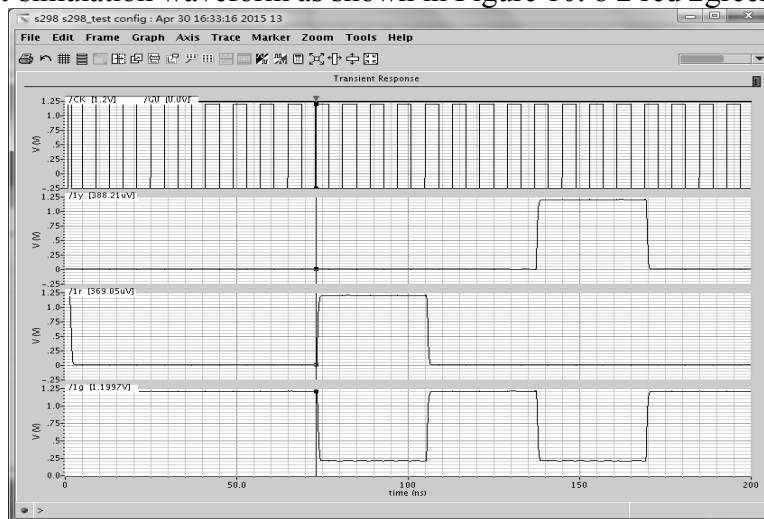

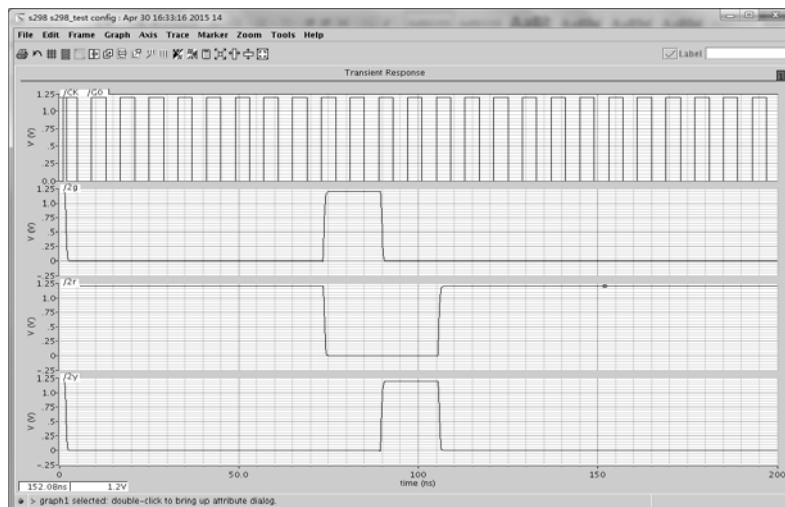Figure 9. G2G1(10) the post simulation waveform of 2th light

Figure 10. G2G1(10) the post simulation waveform of 2th light

Conclusion

In this thesis, the standard cell library building and verification flow based on the SMIC 130nm process were completed, especially the optimization of the 1-bit full adder cell. The structure and layout of the full adder in the SMIC library are analyzed, and after the structure and size of the adder cell were improved, the simulation showed a better result by H-spice. The comparison shows that the optimized adder was not only smaller in the area, with width decreased by 0.82μm, but also had advantages in power consumption and timing, with energy delay product reduced by 7.7%. The s298 circuit in ISCAS Benchmark89 was used as the benchmark to complete the verification method of the standard cell library.

Acknowledgement

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