

Use of Automation in Sensor Readout ASIC Chip Characterization to Improve Test Yield, Coverage and Man-Hour Reduction

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Abstract— An approach for efficient sensor readout ASIC chip characterization is presented in this paper. Use of automation results in better test yield and coverage, in addition to man-hour reduction. In order to perform this, the hardware setup has been integrated based on laboratory bench instrumentation. All of hardware is controlled by software written in VEE PRO graphical programming language.

Keywords—ion sensing electrode; ion sensing field effect transistor; moisture sensor

I. INTRODUCTION

The trend in the chip design verification increases linearly with new products, thus device characterization tests have increased exponentially and created bottlenecks. If there is only one function (herein designated as “A”), “A” need only be tested. If there are two functions, “A” and “B”, then test sets will be “A,” “B,” “AB,” and “BA.” Three functions or more will thus increase the test sets dramatically. Therefore, an automated software testing is the best way to increase the effectiveness of resources and time, tests can be faster, they’re consistent, and test can be run over and over again with less overhead. [2]

This paper elaborates automation setups and methods that replace manual test procedures so that design bottlenecks can be eliminated and device characterization improved in terms of test yield, coverage and man-hour reduction. In achieving the stated objective, it will be necessary to develop a framework that attains and integrates commonality, maintainability, and reusability [3].

Normally, the engineer manually sets up the power supplies, device stimulus, triggers the DUT (device under test), then records multi-meter measurements by hand. This process is tedious, time-consuming, and lends itself to errors. In essence, a typical validation procedure requires the use of three or four different instruments which results in the necessity of different protocols to control the instruments. Therefore, the key goal of this paper is to improve the test methodologies by automating test techniques. The test project should use easy, flexible, modular, interchangeable components. Whenever feasible, the interface screen should match as closely as possible to the actual test measurement instruments. The programming language used is VEE PRO as most of the bench equipment are from Agilent. In the sections that follow, the ASIC chip to be tested (DUT) are first explained followed by the hardware setups necessary to

implement the automated testing. Next the software code and routines that drives the bench equipment are discussed. Finally the conclusion surveys the benefits gains from such an exercise.

II. CHIP ARCHITECTURE

The ASIC to be tested is designed in-house. It provides the following sensor read out circuits:-

- Three channels of individual ion sensing electrode (ISE) sensor readout circuit
- Two ion sensing field effect transistor (ISFET) readout circuit of which either one (mutually exclusive) is used to readout signals from the ISFET sensor.
- One moisture sensor readout circuit.

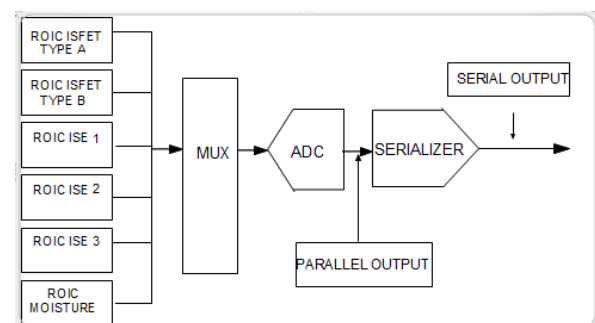


FIGURE I. ASIC CHIP DESIGN ARCHITECTURE

Figure 1 shows the chip design architecture. At any instance in time, only one of these blocks is selected through a multiplexer for connection to an Analog Digital Converter (ADC) through an external low pass filter.

To verify the automation setups, each of these readout circuits has been separately tested manually, which include ISFET TYPE A, ISFET TYPE B, ISE1, ISE2, ISE3, MOISTURE and also ADC tests. The results obtained from the manual tests, are used as reference to verify the performance of the automation routines and its results.

III. EQUIPMENT & SOFTWARE

In order to perform all these testing, either in manual or automated mode, it involves some high end instruments coupled with software as follows:-

- Agilent E3631A Triple Output DC Power Supply
- Agilent 34970A Data Acquisition (3 Slots)
- Slot 1: Agilent 34903A 20 Channel Actuator/General Purpose Switch (ACT)
- Slot 2: Agilent 34901A 20 Channel Multiplexer (MUL)
- Test DUT PCB Board
- National Instrument GPIB/GPIB interface
- Agilent 82357B USB/GPIB Interface
- Agilent VEE PRO software
- Agilent Connection Expert software

The main instruments and software in this automation is Agilent 34903A 20 Channel Actuator/General Purpose Switch, Agilent 34901A 20 Channel Multiplexer, and Agilent VEE PRO software.

Agilent VEE PRO is a graphical programming language designed specifically for test and measurement applications. With this software, instruments can easily communicate with each other and automation is possible. Therefore, the switches can be easily programmed on/off based on the required test.

Agilent 34903A 20 Channel Actuator/General Purpose Switch has 20 independent single-pole, double-throw (SPDT) relays and is used to cycle power to products under test, control indicator and status lights, and to actuate external power relays and solenoids. Combining it with matrix and multiplexer modules allows a custom switch system to be built. In automated mode, it acts as switches and used to sequence the tests. From one test to another, different pins are used. Therefore, so correct pins need to be chosen for a particular test by closing or opening the appropriate switches.

Agilent 34901A 20 Channel Multiplexer is the most versatile multiplexer for general purpose scanning. It acts as the Digital Multimeter in the Automation.

IV. SET-UP CONFIGURATION

As shown in Figure 2, the USB/GPIB and GPIB/GPIB cables are used for communication between computer and instrument and between the instruments. As mentioned earlier, the Agilent 34903A 20 Channel Actuator/General Purpose Switch act are used extensively in the automation procedure.

It is used for setting up different test configurations through automation. In manual testing, different tests will have different pin set-up configuration so when changing from one test to another; pin connection will be different for each test setup. It requires some time to change the set-up and errors are possible especially done manually.

However, in automation mode, all the pins required for all these tests will connect to the 20 Channel Actuator/General Purpose Switch so when performing the particular tests, the pin selection required resulting in closure of particular switches are done through software written in Agilent VEE

PRO. Similar reasoning goes for 20 Channel Multiplexer, connect all the output pins to it so when need to read the output value from the particular pin, just need to close the output value from the particular pin, just need to close the particular switch. This can also perform in the VEE PRO. This is a good instrument when need to read few values from different pin. Instead of using multi-meter to read one by one, by using this instrument all the values can be read automatically one after another. Therefore, with these two instruments, it saves setup and measure time when changing from one test to another.

After setting up all the hardware and software, the program written in VEE PRO is executed. All the results are exported and stored in Microsoft Excel format in the computer.

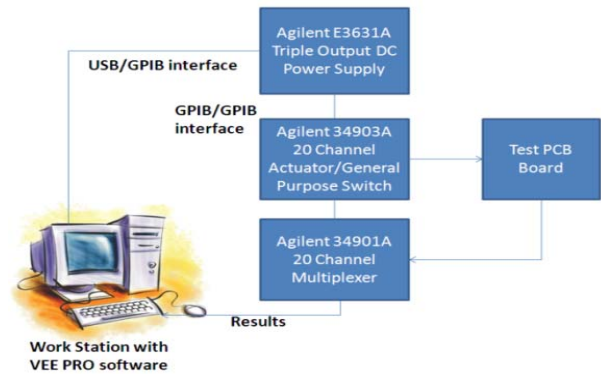


FIGURE II. SETUP CONFIGURATION FOR TEST AUTOMATION

V. FLOW CHART AND VEE PRO PROGRAM

Since all the tests composed of the same hardware and software. The only different thing between them is the channels use in the Agilent 34903A 20 Channel Actuator (which act as the switches to switch between each test). Therefore, the flow chart for each tests are almost the same, only the switches involved different. Figure 3 shows the example of the flow chart for ISE1 test.

The programs written in Agilent's VEE PRO software are based on the flow chart. The commands used in the VEE PRO to communicate with the instruments are called SCPI commands. Figure 4 and 5 show the VEE PRO program for ISE 1 test and also the complete program for all the tests, which include ISE1, ISE2, ISE3, ISFET TYPE A and also ISFET TYPE B.

Figure 5 shows the complete program for the whole automation process which combined all ISE and ISFET tests. In the figure, the 3 gray colour icons include all the ISE tests while the pink colour icons include all the ISFET tests. For example, when the ISE1 icon is clicked, it depicts the Figure 4 program. The Figure 5 program is used to combine all of the tests, so they perform automatically one after another with final results exported and stored in excel format on the computer.

This automation has faster testing time compared to the conventional method. From Table I below, we can see the complete test for one chip takes 2.4 hours compared to 4 minutes when it have been automated. Software testing time

for 80% of the total cost of software development [6] and the cost could be reduced if the process of testing is automated.

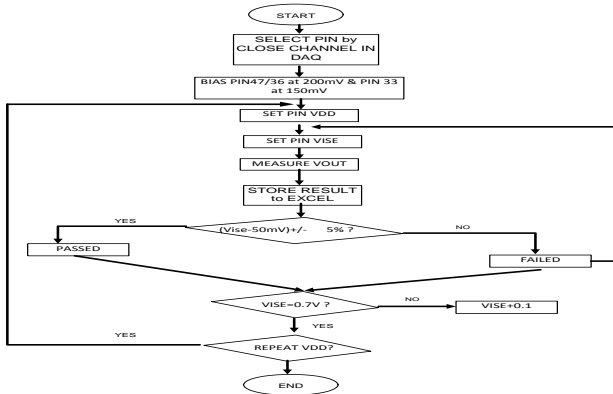


FIGURE III. FLOW CHART FOR ISE1 TEST

TABLE I. MAN-HOUR COMPARISON

Total Chip Tested	Man-hour reduction table		
	Manual	Automation	Total hour save
623	1495 hours	40 hours	1455 hours

VI. ADC ARCHITECTURE

The automation code does not include the ADC and Serializer block. This is because the characterization of the ADC and Serializer will involve AC tests as well as DC tests, as such they do not fit well with the earlier hardware setup where it is for DC tests only. However characterization of the ADC and serializer is done separately and confirmed working before the setup is used to test for functionality of the entire ASIC. Table II below presented the test result for ADC.

In order to perform functionality test, a voltage input was biased at the input port for each ROIC. The input will go through multiplexer, ADC and serializer. The digital output in binary format will then convert to analog value by calculation method. The testing results for some chips were tabulated in Table III and IV.

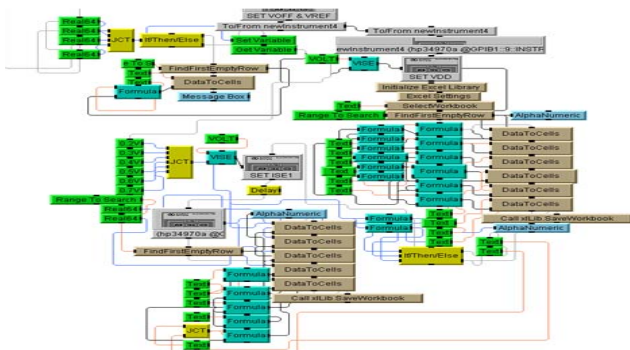


FIGURE IV. VEE PRO PROGRAM ISE N+ TEST

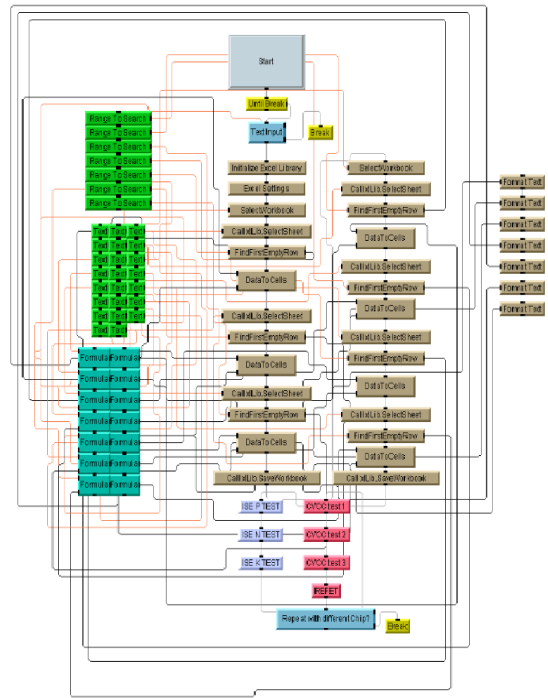


FIGURE V. COMPLETE PROGRAM FOR ALL ROIC

TABLE II. TEST RESULT FOR ADC BLOCK

Chip No.	Result for Open Port Test		
	Input Setup	Serialize Output(binary)	Output (V)
93	0 V	0000100110	0.037
	0.5V	0110110001	0.422
	1 V	1110111001	0.930
51	0 V	0000000010	1.94 m
	0.5V	0110110101	0.426
	1 V	1110111110	0.935
86	0 V	0000011011	0.026
	0.5V	0100111011	0.307
	1 V	1010011111	0.655
C19	0 V	0000100011	0.034
	0.5V	0111001010	0.447
	1 V	1111011010	0.962

TABLE III. TEST RESULT FOR ISFET-REFET ROIC

Chip No.	Result for ISFET-REFET ROIC		
	Input Setup	Serialize Output(binary)	Output (V)
93	0.515 V	0111000101	0.442
51	0.519 V	0111001010	0.447
86	0.423 V	0101001111	0.327
C19	0.513 V	0111010110	0.458

TABLE IV. TEST RESULT FOR ISE ROIC

Chip No.	Result for ISE ROIC		
	Input Setup	Serialize Output(binary)	Output (V)
93	0 V	0000100111	0.038
	0.5V	0101111101	0.372
	1 V	1110000000	0.875

VII. CONCLUSION

A VEE PRO based software for ASIC chip test automation has been presented in this paper. Currently, this is only considered semi-automated since mechanical handling is still required during part change. The ADC and serializer block test are still performed manually. However, even with this setup now, in terms of efficiency and man-hour reduction, significant achievement has been accomplished. This is especially evident when a large batch of prototype chips need to be characterized.

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