A High Energy Resolution X-ray Spectrometer using SDD

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Abstract. A high energy resolution X-ray spectrometer based on Silicon Drift Detector is described in this paper. The spectrometer consists of the SDD detector module, the analog electronics for shaping and filtering and the digital electronics for peak detection and data transfer. The system can working at room temperature as a thermo electric cooler (Peltier Element) is integrated into the SDD chip. The dynamic range is about 1 keV to 10 keV. Test results indicated high energy resolution Full Width at Half Maximum (FWHM), which is better than 160 eV @ 5.9 keV with the incoming photon of radioisotopes (^{55}Fe).

Introduction

The radiation of X-rays are widely used in many fields (such as airport security, X-ray astronomy, X-ray medical, X-ray crystallography, X-ray microscopic and so on) based on its properties [1]. X-rays with photon energies above 5 - 10 keV are called hard X-rays, while those with lower energy are called soft X-rays. A high energy resolution of Soft X-ray Detection (SXD) system is very necessary and useful in scientific experiments and to explor the origin of the universe.
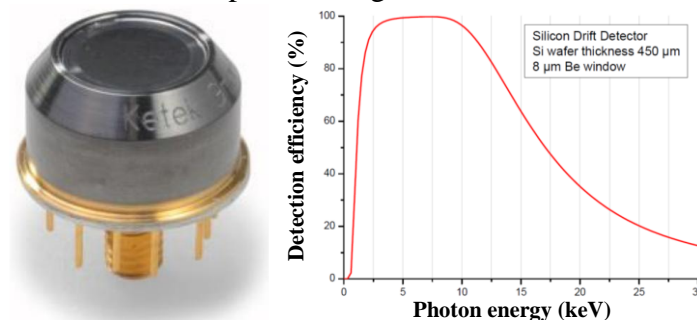

Fig. 1 SDD detector and its absolution efficiency

Silicon Drift Detectors (SDD) are the state-of-the-art X-ray detectors based on silicon substrates. As shown in Fig. 1 is the used detector KETEK VITUS SDD H30 [2] and its absolution efficiency curve (about 70% at 1 keV and 98% at 10 keV), while the detector have 30 mm^2 active area with 8 μm Be window. An incoming photon will generate a number of electrons and holes dependent on its energy. A followed readout electronics based on the SDD will be discribed in the following sections.

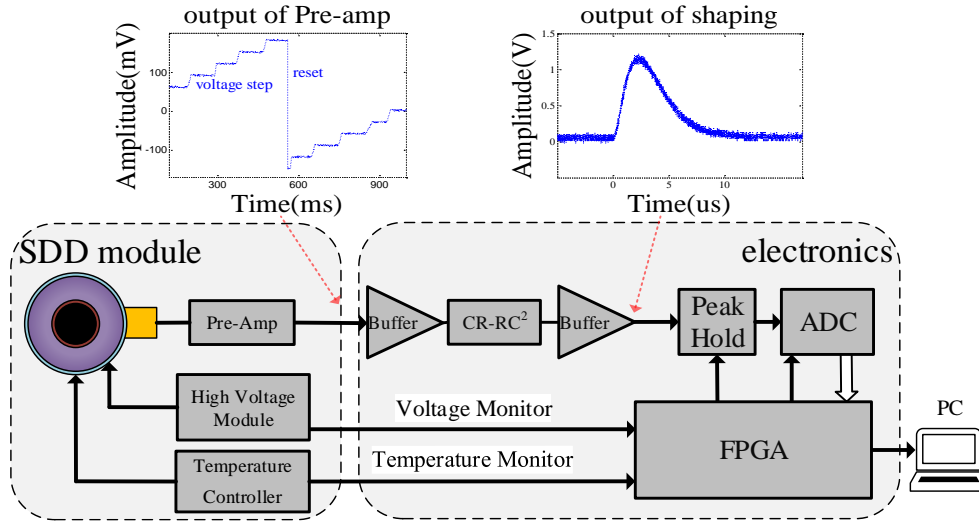## Structure of the readout electronics

Fig. 2 Structure of the SDD based readout electronics

As shown in Fig. 2, is the structure of the readout electronics. The SDD detector is surpported by the High Voltage Module and Temperature Controller to guarantee a good working environment, while the statues of the voltage and temperature were monitored by the Field Programmable Gate Array (FPGA) simultaneously. The output of the SDD is buffered by a low-noise & high-gain Pre-Amp, which is a voltage step well between $\pm$ 2 V because of the reset signal. The output of the Pre-Amp is followed by the CR-RC^2 [3] filter and shaper, after then the quasi-Gaussian output is fed to the Peak Hold module and then be digitalized by a 14-bit Analog to Digital Converter (ADC) (3 MHz sample rate). The digitized results is buffred and packaged in the FPGA, then be readout to remote PC. Detailes will be listed bellow.
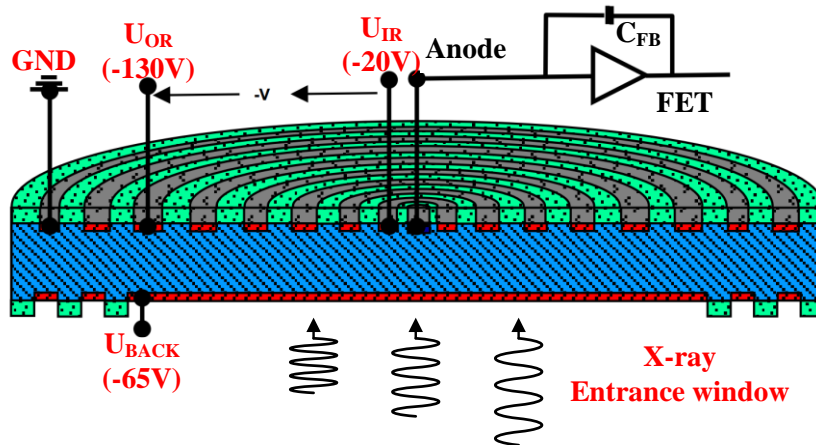
Silicon Drift Detector

Fig. 3 Schematic of SDD chip

As shown in Fig. 3 is the schematic of the SDD chip. The anode of the SDD is connected to a Field Effect Transistor (FET) and Feed Back Capacitance (C_{FB}) which forms the first part of a Charge Sensitive Amplifier (CSA). A certain rise time is dependent on the location of interaction of the X-ray with the SDD chip, while a certain amplitude is dependent on the energy of the incoming photon. SDDs require High Voltages Power Supply (low noise stabilized, U_{OR}'-130V', U_{IR}'-25V', U_{BACK}'-65V',), Preamplifier Module (ultra-low-noise, charge-sensitive, ramped reset type, high-gain) and

Temperature Controller Module (Peltier Element based thermo electric cooler) to guarantee a good working enviroment, meanwhile it is necessary to read out the temperature sensor of the SDD.

Peak-Hold module

One kernel part of the readout electronics is the Peak Hold method, which combine with Analog to Digital Converter (ADC) for peak detection. The peak of the analog quasi-Gaussian output is detected and held by the Peak Hold module, then be injected to ADC for digitization. A high performance peak-hold chip (PH300) was chosen, which was designed for satellite instrumentation (equally useful in laboratory and commercial applications for its stability and characteristics).
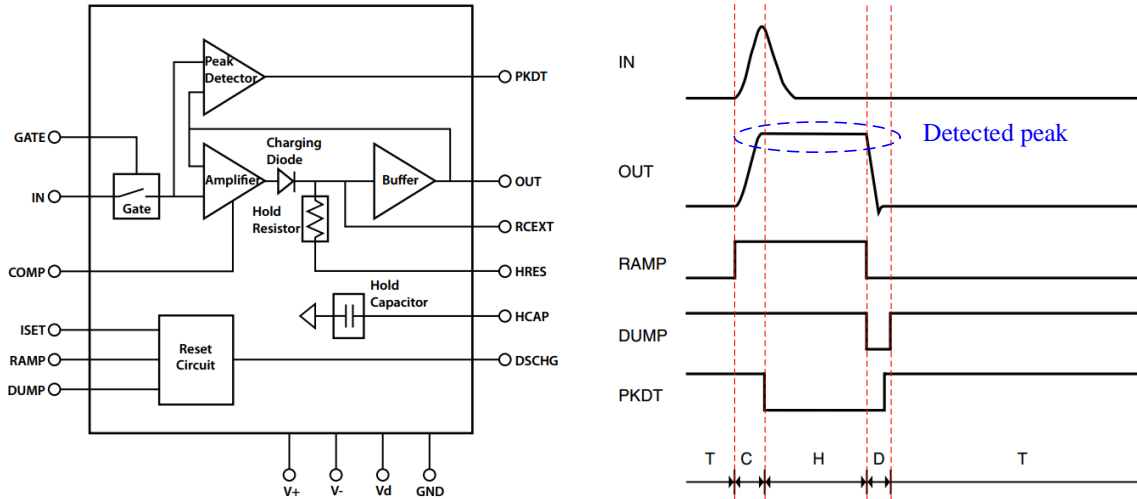

Fig. 4 The Function and Timing diagram of PH300 [4]

PH300 is a peak-hold device, to track an analog input and keep the maximum amplitude as a peak voltage on a hold capacitor. As shown in Fig. 4, the input (marked as 'IN') is sensed by the error amplifier when the Gate is open (High), which is controlled by Transistor-Transistor Loigc (TTL) standard. The hold capacitor is charged though a charging diode and a hold resistor during the rise time of the signal (called charging mode marked as 'C'). Then the device goes into the hold mode (marked as 'H') as soon as the input reaches V_{max} and starts to decay. After completing the sample of the peak, the circuit was in fast discharge (was configured in the application) mode (marked as 'D'), the hold capacitor is discharged through a large current for a short period of time. Finally, the circuit was ready for reciving a new peak, which is called the tracking mode (marked as 'T').

The control signal is generated by the FPGA, which is converted from 3.3 V standard to 5V standard according to a schmitt CMOS 16-bit Bidirectional MultiPurpose Transceiver (UT54ACS164245S). The 'GATE' was set as HIGH in the application. The 'PKDT' was the output of the PH300 when the peak is found and in the holding mode. The 'RAMP' is the input which starts from the rise time of the 'IN', and set as LOW when in the discharge mode. The 'OUT' from PH300 is sampled by a 14-bit ADC (AD9243) with 3 MHz samping rate. The results is buffered and packaged in FPGA, then transmitted to remote PC for further analyzing.

Test results

In order to evaluate the X-ray spectrometer designed in this paper, a test platform was set up, as shown in Fig. 5. The test system is mainly consists of the signal source (AFG 3252), the radioisotope (^{55}Fe), the SDD module and shaping board (marked as 'A'), the digital board (marked as 'B') and power supply module.

Firstly we measure the electronics linearity of the peak hold and ADC module, a series of quasi-Gaussian (generate by signal source AFG3252) were conducted with increasing amplitude

measured by the readout electronics. The input amplitude ranges from 50 mV to 2500 mV with 300 mV interval, which is equivalent to the dynamic range (1 keV to 10 keV).
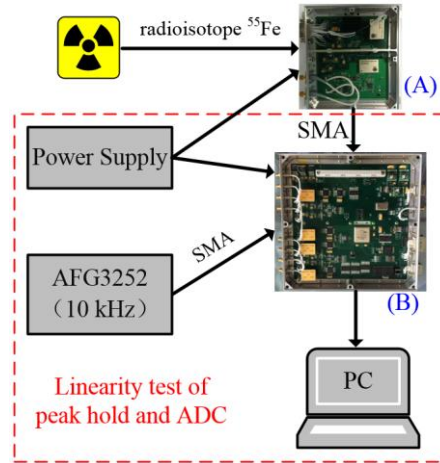

Fig. 5 Test platfrom of the soft X-ray spectrometer

A linear curve is shown in Fig. 6, with an integral non-linearity less than 1%.

After the X-ray spectrometer were assembled, including both the detector and electronics properties. We use the radioisotope (^{55}Fe) as the input of the incoming photon [5].
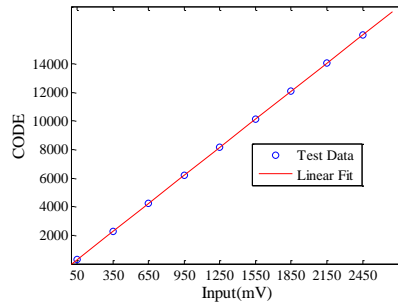

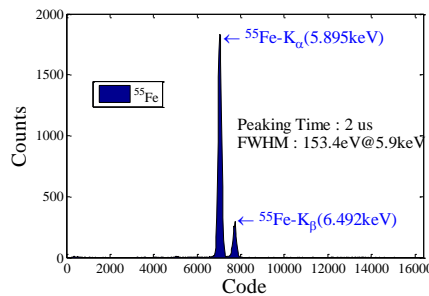Fig. 6 The linear curve of the Peakhold and ADC circut

Fig. 7 The test spectrum using the radioisotope ^{55}Fe

As shown in Fig. 7, the result of energy spectrum indicates that the energy resolution Full Width at Half Maximum (FWHM) is better than 160 eV @ 5.9 keV (using X-ray as the incoming photon for SDD).

Summary

A high energy resolution of soft X-ray spectrometer based on SDD is designed in this paper. Which achives a dynamic range of about 1 keV to 10 keV. The energy resolution (FWHM) is better than 160 eV @ 5.9 keV.

Acknowledgment

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