

FPGA Implementation of Rate Control for JPEG2000

Shijie Qiao^{1, a *}, Aiqing Yi^{1, b} and Yuan Yang^{1, c}

¹Department of Electronic Engineering, Xi'an University of Technology, Xi'an, China

^aqiaoshijie@xaut.edu.cn, ^byiaiqing@163.com, ^cyangyuan@xaut.edu.cn

Keywords: JPEG2000, Rate control, Tier1 coding, Rate distortion estimation, FPGA.

Abstract. This paper presents a FPGA implementation of rate control system for JPEG2000. The input image is discrete wavelet transformed, and the wavelet coefficients are encoded by Tier1 coding with rate distortion estimation. During the process of the Tier1 coding, the bit rate for each code block is allocated and the bit stream is then truncated to produce the final bit stream. The Verilog HDL modules for the rate control system are designed, simulated and synthesized to Altera's FPGA. The result shows that the architecture proposed in this paper is correct.

Introduction

JPEG2000 is a new still image coding standard. It can get high compression performance and supports a rich set of novel functions [1]. In JPEG2000, the rate control algorithms, called PCRD [2] is used to truncate the bit stream produced by Tier1 coding. Since the PCRD algorithm is processed after Tier1 coding, in lower bit rate, lots of the encoding passes in Tier1 coding are discarded from the final bit stream. To reduce the computation redundancy of PCRD in lower bit rate, several rate control algorithms have been proposed, such as algorithms described in paper [3] and [4].

In this paper, we present a FPGA implementation of rate control system for JPEG2000. The input image is discrete wavelet transformed, and the wavelet coefficients are then encoded by Tier1 coding with rate distortion estimation. During the process of the Tier1 coding, the bit rate for each code block is allocated, and the bit stream is then truncated to produce the final bit stream. The Verilog HDL modules for the rate control system are designed, simulated and synthesized to Altera's FPGA. The generated programming file is downloaded to the FPGA and tested in system. The test result shows that the architecture designed in this paper is correct.

This paper is organized as follows. The architecture of the rate control system for JPEG2000 is presented in section 2. In section 3, the Tier1 encoding with rate distortion estimation is proposed. The rate control and bit stream truncation are given in section 4. The rate control system is implemented with FGPA in section 5. A conclusion is present in section 6.

Architecture of Rate Control for JPEG2000

The architecture of the rate control system for JPEG2000 is show in Fig.1. Under the control of the controller module, the input image is discrete wavelet transformed (DWT) by DWT module, the wavelet coefficients are then stored in the DWT RAM and encoded by Tier1 coding module. The bit stream produced by Tier1 coding is collected by the bit stream buffer. During the process of the Tier1 coding, the rate control module is used to allocate bit rate for each code block and the bit stream is then truncated by the bit stream truncation module to produce the final bit stream.

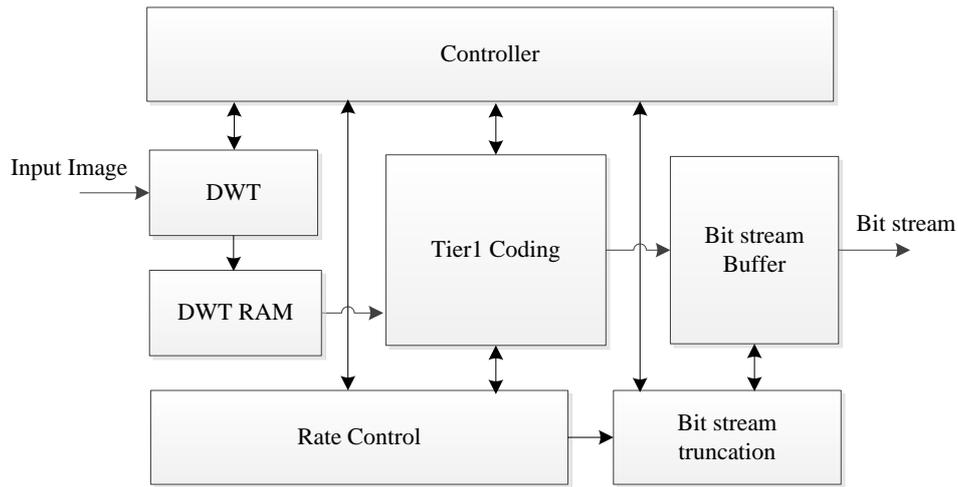


Fig.1 Architecture of rate control for JPEG2000

The controller is the main control module of the rate control system and is implemented by state machine. The state machine for the controller is showed in Fig.2. When the coding system starts up, the state machine stays in the idle state, when the coding enable signal goes high, the state machine changes its state to the initialization state, all registers in the coding system are set to the default value in this state. After initialization, the state machine changes its state to the state named DWT, the data of the image is then wavelet transformed by DWT module in this state. After DWT, the state is changed to the Tier1 coding state, in this state, the wavelet coefficients are encoded by bit plane coding and arithmetic coding. During the process of Tier1 coding, the state machine changes its state between Tier1coding state and rate control state, the code block is encoded and the bit rate for the code block is allocated. Once all code blocks are encoded, the state machine changes its state to truncation state, the bit stream produced by Tier1 coding is then truncated and the final bit stream is outputted from the system. In the next cycle, the state is changed to idle state to wait for encoding the next image.

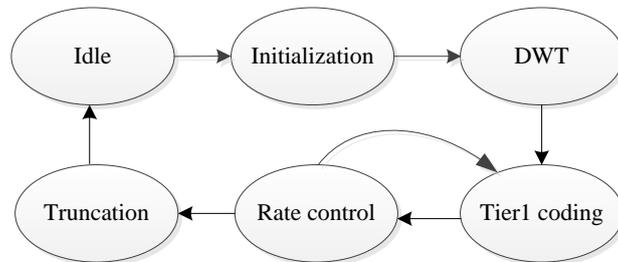


Fig.2 The state machine for the Controller

The Tier1 coding with rate distortion estimation, the rate control and bit stream truncation are given in the following sections. The architecture for DWT is not included in this paper, for hardware implementation of DWT, please refer to the paper [5].

Tier1 Coding with Rate Distortion Estimation

The Tier1 coding is the main coding procedure in JPEG2000. In paper [6] we proposed a hardware architecture for Tier1 coding. The architecture contains two coding blocks, the bit plane coding and arithmetic coding. The bit planes of the wavelet coefficients in each code block are encoded with three coding passes, i.e. the significant propagation pass (SPP), the magnitude refinement pass (MRP) and the clean-up pass (CUP). The symbols CX (context) and D (decision) produced by the bit plane coding are then coded by arithmetic coding, named MQ.

In order to reduce the computation redundancy, the rate control algorithm is implemented during the process of the Tier1 coding. To implement rate control, two variables must be available to

calculate the rate distortion slope, one is the decrease of distortion ΔD , and the other is the increase of the number of code bytes ΔR . In this paper, we add three function modules to the architecture of Tier1 coding, one is for distortion estimation, another is for the increase of the number of code bytes, and the third one is for rate distortion slope calculation. The architecture of Tier1 coding with rate distortion estimation is showed in Fig.3. For detailed information about bit plane coding and arithmetic coding, please ref to the paper [6].

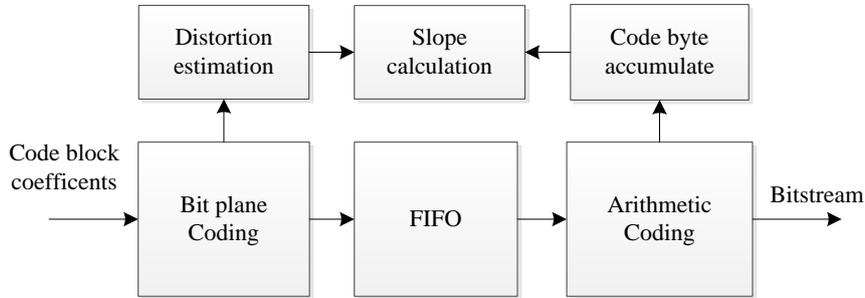


Fig.3 Tier1 coding with rate distortion estimation

The distortion information of three coding passes in bit plane coding is provided by the distortion estimation module. The architecture for distortion estimation is showed in Fig.4. According to the bit plane information and the type of the coding passes, the distortion information is read from one of the two distortion tables. The significant coding distortion table is for SPP and CUP, and the magnitude coding distortion table is for MRP. The distortion are accumulated by the adder and then registered in the D flip flop. The distortion FD outputted from D flip flop is used to calculated the decrease of distortion ΔD , the ΔD is stored in register.

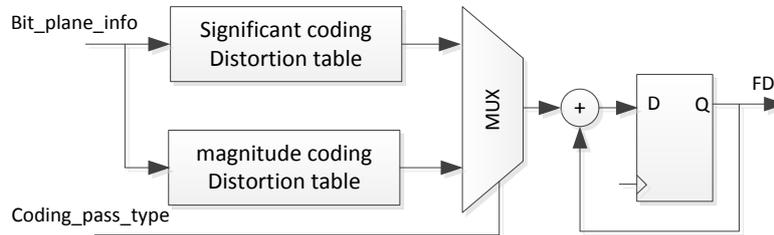


Fig.4 The architecture for distortion estimation

The module named code byte accumulation is used to accumulate the number of code bytes generated by the arithmetic coding. The number of code bytes are then stored in the rate distortion table, the increase of the number of code bytes ΔR for the coding passes are then calculated and stored in register. Once the ΔR and ΔD are ready, the rate distortion slope S_k is calculated by the slope calculation module and stored in the rate distortion table too.

Rate Control and Bit Stream Truncation

The rate distortion table is used to store the number of code bytes and the rate distortion slopes, as described in the previous section. The rate distortion slops stored in this table is in descending order. Other information, such as subband index and code block index are also stored in this table.

During the process of the Tier1 coding, the minimal slop discarding methods [7] is used to allocate bit rates for different code blocks and coding passes, and the optimal truncation point S_{opt} is obtained. Each S_k is compared with S_{opt} , once the $S_k < S_{opt}$, all bit stream after the S_k are then discarded, the bit stream between the start_addr and the stop_addr are truncated and outputted from the bit stream buffer as showed in Fig.5.

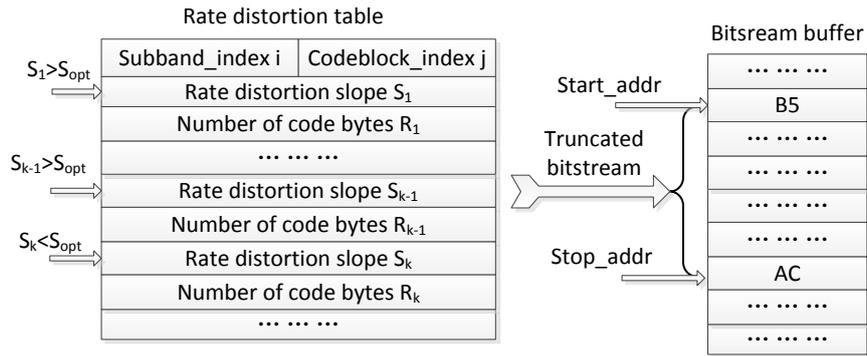


Fig.5 The structure for bit stream truncation

FPGA Implementation of Rate Control System

The Verilog HDL modules for the architecture are designed and simulated. The simulation result shows that the bit streams outputted from the architecture are the same as the bit streams outputted from the C programs. Part of the simulation result is showed in Fig.6.

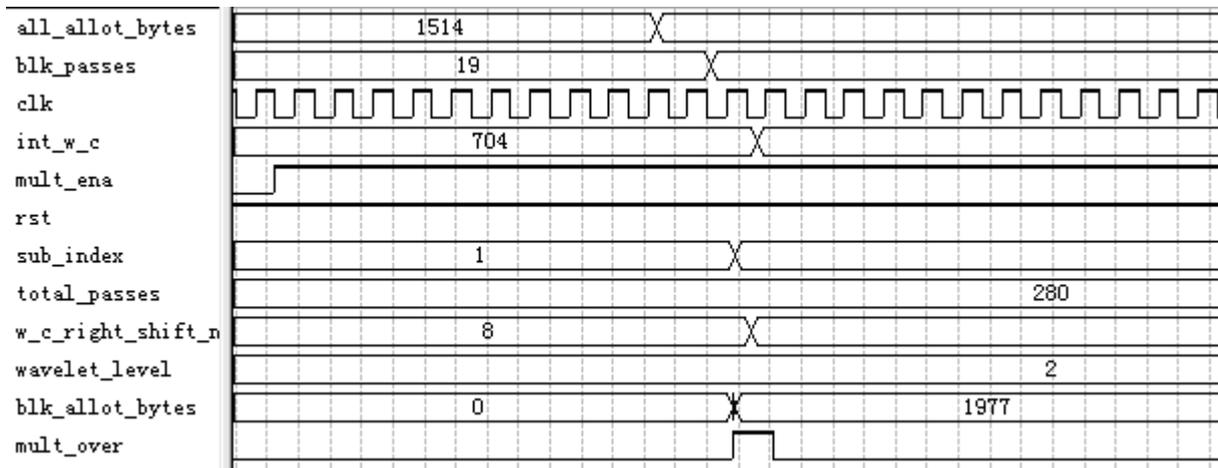


Fig.6 Part of simulation result for rate control system

The architecture is then synthesized to Altera's FPGA by QuartusII, the Cyclone II device EP2C35F672C8 is selected, and the synthesized result shows that the clock of the system can be up to 70.8 MHz. After place and route in QuartusII, the generated programming file is downloaded to the FPGA and tested in system as show in Fig.7. The test result shows that the architecture designed in this paper is correct.

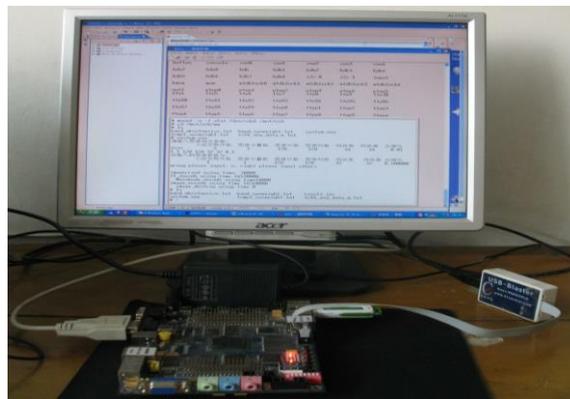


Fig. 7 FPGA implementation of rate control system

Conclusion

In this paper, we present a FPGA implementation of rate control system for JPEG2000. The input image is discrete wavelet transformed, and the wavelet coefficients are encoded by Tier1 coding with rate distortion estimation. During the process of the Tier1 coding, the bit rate for each code block is allocated, and the bit stream is truncated to produce the final bit stream. The Verilog HDL modules of the architecture are designed, simulated and synthesized to Altera's FPGA. The generated programming file is downloaded to the FPGA and tested in system. The test result shows that the architecture designed in this paper is correct.

Acknowledgments

This work is supported by Science and Technology Planning Project of Xi'an, China (No.CXY1436 (4)).

References

- [1] ISO/IEC 15444-1, JPEG2000 Image encoding system. Part1: Core coding system, 2002.
- [2] D. Taubman, High Performance Scalable Image Compression with EBCOT. IEEE Transaction on Image Processing. vol. 9, pp.1158-1170, 2000.
- [3] T. Kim, H. M. Kim, P. S. Tsai. T. Acharya, Memory Efficient Progressive Rate-Distortion Algorithm for JPEG 2000, IEEE Transactions On Circuits and Systems for Video Technology, Vol. 15, pp.181-187, 2005.
- [4] Z. Z. Wu, N .N. Zheng, Efficient Rate-Control System With Three Stages for JPEG2000 Image Coding, IEEE Transactions On Circuits and Systems for Video Technology, Vol. 16, pp.1063-1073, 2006.
- [5] K. Mei, N. N. Zheng, H. van, D. Wetering. High-speed and memory-efficient VLSI design of 2D DWT for JPEG2000, Electronics Letters, vol. 42,pp.907-908, 2006.
- [6] S. J. Qiao, Y. Yang. Hardware Implementation of Tier1 Coding for JPEG2000, Proceedings of the 2012 International Conference on Information Technology and Software Engineering, pp.657-663, 2013.
- [7] T. H. Chang, L. L. Chen, C. J. Lian, H. H. Chen, L. G. Chen, Computation reduction technique for lossy JPEG2000 encoding through EBCOT tier-2 feedback processing, Proc. IEEE International Conference on Image processing, pp.85-88, 2002.