Research on Self-biased PLL Technique for High Speed SERDES Chips

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Abstract. This paper is designed for wide input range of SerDes chip phase-locked loop circuit, using self-biased technology, there is a wide range of input reference frequency, the need for external bias circuit, and loop bandwidth can follow input reference frequency changes in noise with good inhibitory effect. Small footprint annular VCO wide frequency adjustment range, and can easily produce the CDR SerDes required multi-phase clock.

1. Introduction

Phase-locked loop has been widely used in electronics and communication field, generally used for phase-locked frequency synthesis and clock recovery circuit. All along, it is also a variety of serial-based deserializer chips, the core circuit, responsible for sending and receiving data synchronization, frequency, frequency range and jitter performance quality of its output directly related to the SerDes chip functions [1] [2].

A typical CMOS CPPLL including PFD phase circuit, charge pump, loop filter, VCO), divider. In the phase-locked loop implementation process, often encounter a charge sharing, current mismatch, charge injection and clock feedthrough and other issues [3]. To this end, we design a stable, low noise charge pump is to improve the performance of the key phase-locked loop.

For typical charge pump PLL charge pump current ICH, VCO gain K_{VCO}, and loop filter impedance R are constants, then CPPLL it has a fixed attenuation factor and loop bandwidth, fixed loop bandwidth will limit CPPLL operating frequency range. Therefore, this design proposes a self-biased PLL structure, shown in Figure 1[4].

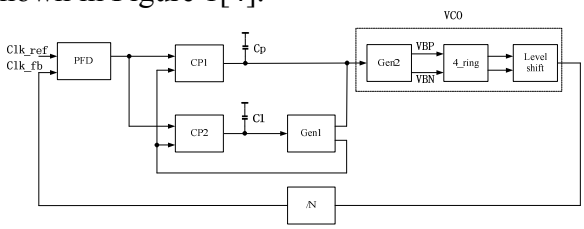

Figure 1 Serdes circuit self-biased PLL structure

Such circuit structure compared with typical CPPLL: make open-loop gain and output frequency dependent, CP current and VCO each stage tail current into a certain ratio between; a loop filter in series with the capacitor impedance is not adopted in the form of fixed impedance, but with a bias circuit in the VCO 1 / g_m impedance[5], whose value is proportional to the output clock cycle; Unlike typical CPPLL driven using a single CP RC network[6], but with two identical, respectively, to CP drive capacitance and resistance, pressure drop summation in VCO bias circuit[7].

VCO phase-locked loop design is a critical module, under normal circumstances, can be divided into two types of LC oscillators and ring oscillators [8]. LC oscillator has a good noise performance, it can produce a high frequency oscillation clock, but there is a large footprint, easy to integrate and limited adjustment range of shortcomings, mainly used in high-speed optical fiber communication clock recovery circuit and RF frequency synthesizer; the ring oscillator and the phase noise characteristics although relatively poor, but with a small footprint, the advantages of wide frequency adjustment range, and can easily generate multi-phase clocks, herein is used in this way.

This paper from the PLL functionality for the analysis of the impact of SerDes chip, based on self-biased technology, using a ring oscillator, designed to meet a frequency range of 1.6-2.7GHz SerDes chip phase-locked loop circuit.

2. Circuit Design.

2.1 Theoretical basis self-biased PLL

For a typical CPPLL, charge pump current ICH, VCO gain KVCO, and loop filter impedance R are constants, then CPPLL it has a fixed attenuation factor and loop bandwidth, fixed loop bandwidth will limit the operating frequency CPPLL range. Compared with typical CPPLL for less than this circuit structure of a typical CPPLL existence there are three important differences:

(1) In order to make the open-loop gain and output frequency dependent, CP current and VCO each stage tail current into a certain proportional relationship.

(2) The impedance of the loop filter instead of using the form of a fixed capacitor in series with an impedance, but with a bias circuit of the VCO 1 / gm impedance, whose value is proportional to the output clock cycles.

(3) is different from the typical use of a single CP CPPLL to drive an RC network, but with two identical capacitors, and CP, respectively, to drive the resistor, the voltage drop generated in the VCO bias circuit summed.

2.2 Design of charge pump

The main function of the charge pump is taken from the PFD to the UP and DOWN convert the digital signal to an analog signal to control the voltage controlled oscillator VCO frequency, that is converted into a control voltage phase error signal. In the actual charge pump circuit design process, we must note that many factors affect the non-ideal. These factors include CP's non-ideal leakage current, current mismatch, charge sharing effect, the charge injection effects. It is because of the presence of these non-ideal effects, leading to appear on the VCO control voltage ripple, thereby causing the output signal jitter.

The traditional charge pump circuit charge-sharing effect, you can use "bootstrap" approach to eliminate, its implementation is to add a unity gain amplifier in the circuit, so that the drain pipe is maintained at the current source control voltage on the output potential. Compromise consider this approach is that, in order to make the circuit can be good work, the op amp should have a greater common-mode input voltage and output voltage range, which will increase the complexity of the circuit and the layout area is large.

Fully differential charge pump has good linearity, noise suppression ability, speed advantages. This design uses the structure shown in Figure 4, the structure is simple, fast switching speed, and switches are all N-type MOS transistor, the load symmetry is very good, relatively high input reference frequency locked loop generally use this structure charge pump.

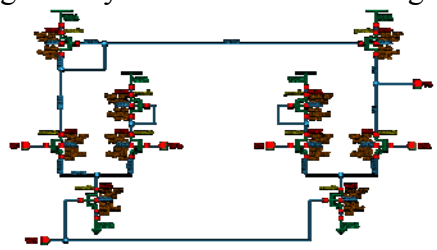

Figure 4 The actual charge pump circuit

2.3 Design of the low-pass filter LPF

The loop filter capacitors and resistors on the pressure drop is generated respectively, by two entirely consistent CP circuit to drive, final control voltage generated by the two summation.

$$R = \frac{y}{2g_m} = \frac{y}{2\sqrt{2kI_D}}$$

As can be seen, the resistance R is inversely proportional to the rms current ID, MOS diode may be connected with a tube as a load, and under the bias current ID, in order to obtain small-signal

equivalent impedance of 1 / gm resistor. Combined VCO bias generating circuit, the voltage summing capacitor and resistor to obtain VCO control voltage VBP and VBN, shown in Figure 5. Based on third-order CPPLL analysis, you can then add a small capacitance CP of the filter to become the second order, in order to produce a more stable control voltage.

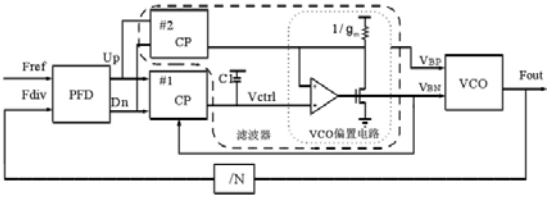

Figure 5 loop filter implementation

2.4 voltage controlled oscillator VCO

Differential buffer with symmetrical load

Symmetric load swing upper PMOS transistor is connected in parallel through a diode of a PMOS bias of the same size pipe implemented (upper swing limit) is the power supply voltage VDD, the lower limit of swing (lower swing limit) is the bias voltage of the PMOS VCTRL. Although symmetrical load is non-linear, but can provide high dynamic power supply noise suppression, non-linear load resistance will usually converted to common mode noise differential mode noise and then the impact of the delay buffer. However, when using symmetric load, a first-order nonlinear coupling noise is canceled out, leaving only the higher-order terms, it can significantly reduce the jitter caused by the common-mode noise.

VCO design

VCO phase-locked loop design is a critical module. For the phase-locked loop, the ability to output clock signal is low-noise design has been pursuing the goal, but the noise performance of the PLL VCO largely determine the performance of the output clock, and the overall design of the loop to crucial influence.

Normally, the oscillator can be divided into two kinds of LC oscillators and ring oscillators, LC oscillators have a good noise performance, it can produce a high frequency oscillation clock, but there is a large footprint, and the adjustment range is not easy to integrate limited drawbacks, mainly used in high-speed optical fiber communication clock recovery circuit and RF frequency synthesizer; and a ring oscillator phase noise characteristics, although relatively poor, but with a small footprint, wide frequency adjustment range of advantages and can be easily The multi-phase clock generation, this paper is used in this way, the overall structure shown in Figure 6.

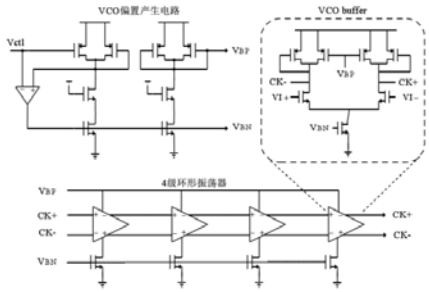

Figure 6 self-bias VCO Chart

Table 1 on-time measurement measurement finesim locking

Fref	UP	DN
80M_tt	0.32ns	0.36ns
100M_tt	0.33ns	0.36ns
135M_tt	0.35ns	0.38ns
135M_ss	0.54ns	0.57ns
135M_ff	0.24ns	0.26ns

3. circuit simulation

PFD mainly for transient simulation, lead-time measurement completion locked.

Measuring method: to build a separate PFD + CP + lpf, the reference clock and feedback divider plus the same clock frequency.

Note: The on-time --up, pulse width down signal

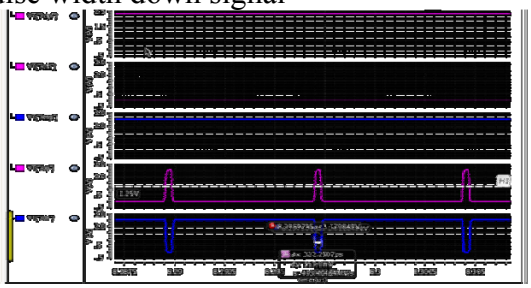

Figure 7 turn-on time 33ns @ 135MHz

According to Figure 7 can be drawn at each process corner, the output current is less than 1uA mismatch region as shown in Table 2. This range determines the VCO center frequency corresponding VCO control voltage range, VCO angle under various process control voltage voltage range can also be determined by this method.

Table 2 charge pump output voltage range under all process corners (Mismatch current is less than 1uA)

	I_{CP}	output voltage Vmin	output voltage Vmax
FF	167.5uA	1.66v	1.72v
TT	125uA	1.65v	1.74v
SS	90.8uA	1.63v	1.76v

4. Summary

From the design of wide-input range of the phase locked loop circuit, adopting self-biased technology, noise has a good inhibitory effect. Small footprint annular VCO wide frequency adjustment range, and can easily generate multi-phase clocks CDR serdes required, designed to meet a frequency range of 1.6-2.7GHz SerDes chip phase-locked loop circuit.

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