A Design and Implementation for Heart Sound Detection Instrument based on FPGA

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Abstract. According to the problem that traditional heart detection equipment is bulky and expensive, approach to designing and implementing portable heart sound detection instrument is proposed in this paper. After the heart sound signal is filtered and amplified by hardware circuits and FPGA, the SCM receives the pre-denoised signal and calculates the heart rate, broadcasting the result in time. Experiments show that the instrument is convenient for patients to diagnose by themselves and make patients receive treatment without delay, which improves the timeliness and accuracy of cardiac auscultation.

Introduction

The traditional phonocardiograph has limitations of heart sound storage and processing for lack of quantitative analysis function [1]. With the development of digital technology, research on heart sound, including heart sound detection, analysis, and identification as well as clinical application has been a hot spot across the world [2, 3]. A large number of achievements involved with heart sound have emerged so far. Many results indicate that the filtering and envelope extraction is the key to system performance [4].

In this paper the method to design and implement the heart sound detection instrument is introduced. The system can not only analyze heart sound signal in time and frequency domain, but also broadcast the testing results in time. The flexibility, portability and reliability make the heart sound detection instrument practicable.

Design of the Integral System

The heart sound is induced by the vibration of myocardial contraction, heart valves closure and blood impacting ventricular wall and artery wall. There are four kinds of heart sound during a period of heartbeat. The first and the second heart sound can be heard in principle. The heart sound signal is weak and unstable with low frequency.

During the heart sound acquisition process, noise cannot be avoided [5]. Such noise has effect on the heart sound analysis. Main noise includes disturbance of 50Hz power frequency and harmonic component, electrode contact noise resulted from breath and motion, muscle contraction noise and electronic device noise. These noises can be reduced to a great extent by taking action. Measures merely relying on hardware circuits are unable to eliminate noise disturbance. Digital filtering technology is indispensable for decreasing noises. Wavelet denoising and self-adaption filter has been used in this paper in order to improve the signal to noise ratio [6].

Low frequency approximation signals and detail signals except for high frequency signals on the scale of 2^5 as the input signal $\mathrm{d}(t)$, including heart sound signal overwhelmed by noises $\mathrm{s}(n)$ and other interference elements $v(n)$. That is to say $\mathrm{d}(t)=s(t)+v(t)$. The reference input signal $\mathrm{x}(t)$, which is independent of $v(t)$ but related to $s(t)$, can be selected from detail signals on the scale of 2^5.

The reference input signal is $X=\left[x_n,\ x_{n-1},\cdots x_{n-p}\right]^T$. The weight vector is $\omega=\left[\omega_1,\ \omega_2,\cdots\omega_p\right]^T$. The output signal is $y(t)=\sum_{k=0}^{p-1}\omega(k)x(t-k)=\omega^T X$ and the error signal is $e(t)=d(t)-y(t)$. Weight is gradually updated by LMS algorithm [14], $\omega(t+1)=\omega(t)+2\mu e(t)X$ (μ is the control factor of self-adaption convergence velocity and stability).

The self-adaption filter follows the principle that the mean square value of error signal $E\left[e_n^{\ 2}\right]$ is the minimum value so that $E\left[y(t)-s(t)\right]=min$. In other words, the filter output $y(t)$ is approaching $s(t)$, not containing disturbance component $v(t)$.

The specific flow chart is shown in Figure 1:

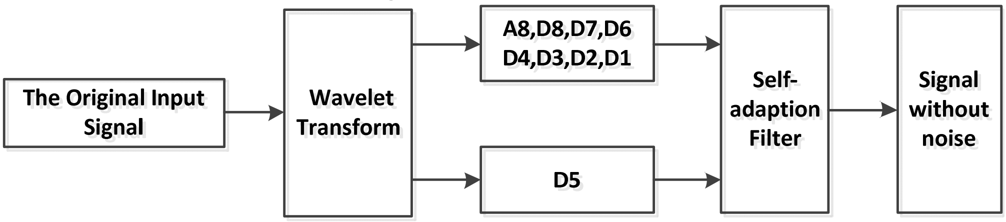


Figure 1. Self-adaption wavelet transform

In general, the heart sound detection instrument is an intelligent signal disposal system. The construction consists of the front hardware circuits realizing the acquisition, filtering and amplification function and microcomputer control part accomplishing data analysis, disposal and output. The two parts cooperate with each other in order to realize the integral system functions. The system schematic diagram is displayed in the Figure 2:

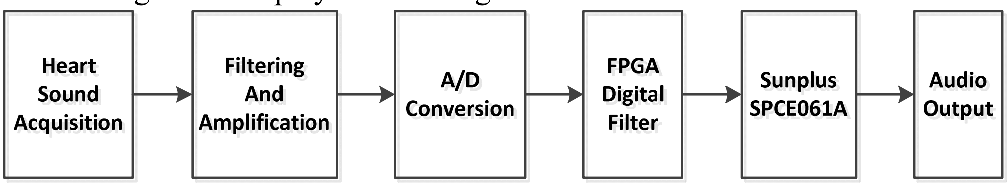


Figure 2. The system schematic diagram

The filtering and amplification module is composed of Butterworth second order low pass filter and two amplifiers LM324. The frequency of useful heart sound is between 0.05Hz and100Hz so that the cutoff frequency of filter is 100Hz. The amplification multiple of each LM324 is 10. It is significant for heart sound detection instrument to measure the heart rate precisely. Therefore hysteresis comparison circuit based on ultra-low offset voltage operational amplifier OP07 is adopted for the sake of transforming heart sound signal into rectangular pulse signal, which can be read by SCM pins to calculate the heart rate conveniently.

The digital filter based on FPGA dispose signals in frequency domain. The signals acquired can be analyzed in the form of frequency spectrum so that noises are able to be separated from the useful signals. However, this approach is only suitable for the situation that the frequency spectrums of useful signals and noises do not overlap. In fact, the frequency spectrums of signals and noises acquired by sensors are usually overlapping. In consequence, the classic method does not work in this case. The nonlinear filtering method based on wavelet transforms can solve the problem above effectively. In wavelet transform domain, the goal of eliminating noises can be achieved through nonlinear processing such as analyzing wavelets multiply, cutting wavelet coefficients and threshold disposal. This kind of denoising method can avoid the loss of information in high frequency to some degree compared to the classic method.

The wavelet coefficients resulted from wavelet analysis can achieve a maximum value, increasing with the growth of decomposition scale, and finally come to a peak value. Nevertheless, noises possessing negative singularity make their characteristics against with the useful signals. The maximum value of wavelet coefficient gradually decreases with the growth of decomposition scale and distributes uniformly in each layer. Taking this trait into consideration, the wavelet transform can realize the separation of signal and noise in both time and frequency domains.

The hardware realization is limited by tremendous calculation of wavelet denoising. FPGA with high integration level and abundant hardware resources makes the hardware realization of wavelet algorithm possible. FPGA uses full parallel structure can dispose data in the form of pipeline, which is different from sequential execution and serial operation of DSP. The wavelet denoising process can be completed efficiently. The thought of distributed algorithm is transformed into LUT (lookup table) in ROM so that the calculation rate can be improved greatly.

The denoising process can be divided into the following three steps: First is the wavelet decomposition. Find an optimal wavelet basis and decompose the signals containing noise. Then high frequency coefficients and low frequency coefficients in N levels can be achieved. Second, threshold processing should be done to the high frequency coefficients. The wavelet ought to be reconstructed thirdly. Reconstruct the low frequency coefficients and high frequency coefficients processed level by level, compounding the denoising signal.

In practical design and implementation, XC3S500E FPAG of spartan3E produced by XILINX Corporation is used to realize the digital filter. AD7482 is chosen as the AD converter and MT48LC8M16A2 from Micron Corporation is used as SDRAM (synchronous dynamic random access memory) for storage. The FT245R chip produced by FTDI used in USB conversion is also necessary during data transmission. Signals are turned into digital signals after AD sampling. Then data are transmitted into FPGA through IO ports. The wavelet processing module in FPGA starts subsequently and convey to next circuit.

The Sunplus SPCE061A SCM has an advantage over processing information. High speed calculation provides condition for broadcasting, combining and recognizing voice. The voice processing is divided into A/D conversion, coding, storage, decoding and D/A conversion parts, which is shown in the following Figure 3:

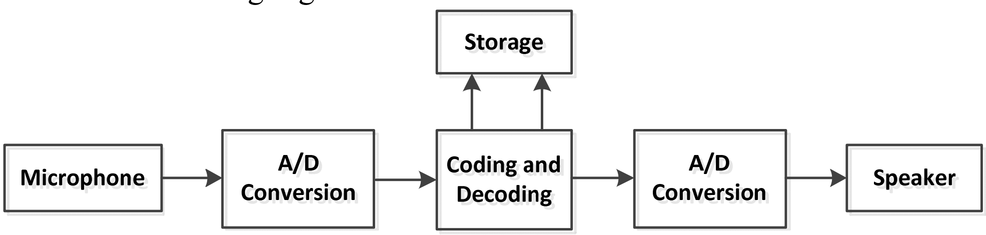


Figure 3. Voice processing in SCM

The Sunplus SPCE061A SCM can solve the problem that WAVE files produced by microphone take up huge storing space by SACM-LIB. Functions such as A/D conversion, coding and decoding are made into modules in this library and each module has its own API (application program interface). Therefore, understanding function and parameters of each module and calling corresponding function can realize relevant impacts.

The integral program follows the principle of modularization design, consisting of many subprograms such as IO ports, data storage, heart rate calculation and voice broadcast programs. The flow chart of main program is shown in Figure 4:

The final program realizes the following functions. The main program first scans the keyboard. When Key 1 has been set, the warning tone begins to be broadcast. Then the system prepares to detect heart sound. At the same time, the timer starts to time for 30 seconds. The counter records the number of heartbeat pulses during this period. When time is up, the counting program will be interrupted. After that the main program doubles the number of heartbeat pulses and divides the value by 10 in order to take the remainder. Finally, the single digits and decimal digits can be broadcast.

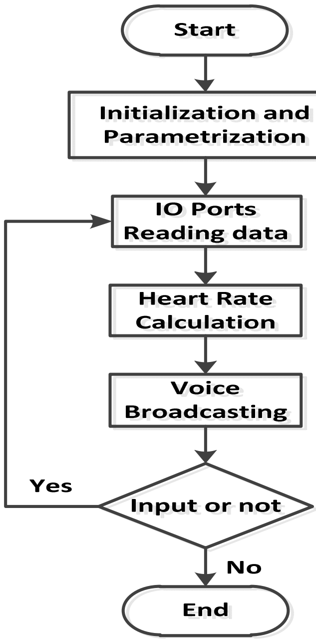
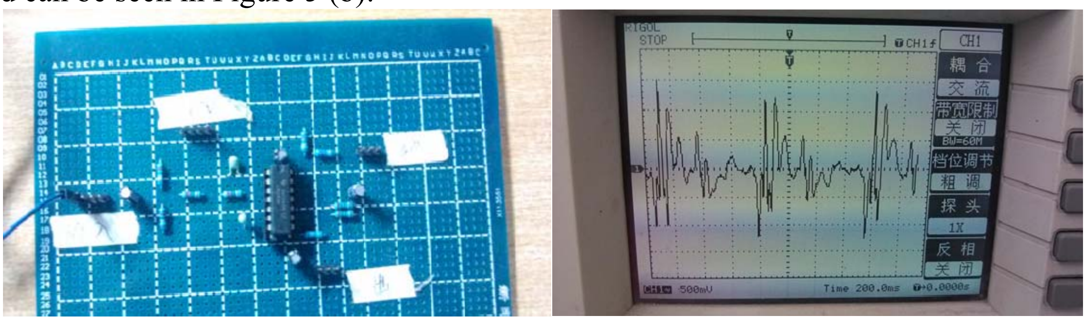


Figure 4. The main program flow chart

Test results

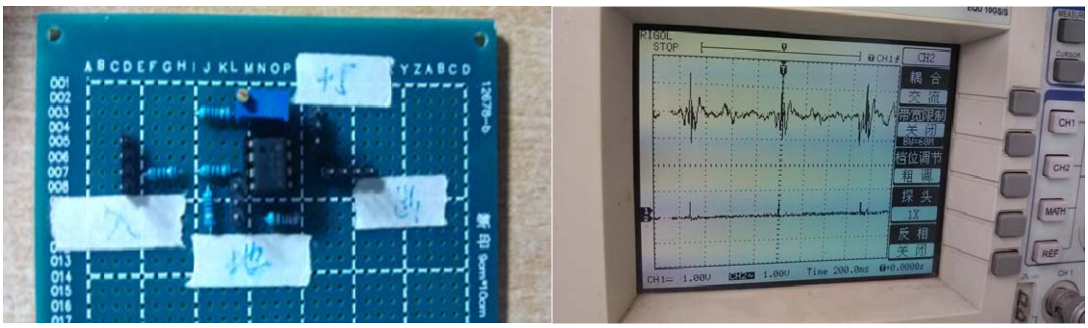
The filtering and amplification circuit is shown in the following Figure 5 (a). The filter is on the left of circuit board. The right side part is the amplifiers. The heart sound signal after filtered and amplified can be seen in Figure 5 (b):



(a) The filtering and amplification circuit (b) The filtered and amplified signal

Figure 5. The filtering and amplification module

The hysteresis comparison circuit centering on the OP07 is displayed in the following Figure 6 (a). The rectangular pulse signal corresponding to the wave crest is also shown in the following Figure 6 (b).



(a) The hysteresis comparison circuit (b) The rectangular pulse signal

Figure 6. The hysteresis comparison module

The integral hardware circuit is shown in Figure 7:

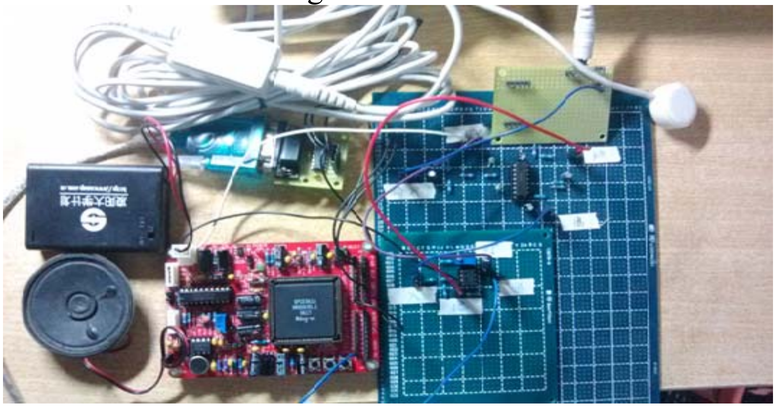


Figure 7. The integral hardware circuit

Conclusion

At present, the heart sound detection technology has been widely used in clinical diagnosis. Plenty of experience indicates high detection accuracy and convenience of this technology. This paper focuses on hardware research and software development of heart sound detection instrument. In accordance with the parameters of instrument requests, the hardware circuit diagrams combine with amounts of relevant information. Besides, modularization design is applied to software parts, which makes the program concise and clear. In order to observe the condition of heartbeat more directly and complete the system function further, the display module can be added into the basic system in the future.

Acknowledgement

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