The Design of AGC Circuit Based On the Variable Gain Amplifier AD603

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Abstract. AGC, Auto Gain Control, is a very important design module in HF transceiver. AGC makes fearfully important effect on improving receive range of receiver and overcoming near-far effect of wireless link. This paper discusses in detail the idea and method of project design of the AGC circuit, affording actual measurement performance index.

Introduction

When shortwave communication received signal, due to the different changes in the ionosphere and the received signal fading conditions, the antenna input level is varied over a wide range [1]. Thus the output signal intensity of the receiver changes greatly. Meanwhile, the output level of the receiver have largely controlled by the volume potentiometer, so that the design of high frequency(HF) modem input signal level control has become an important aspect of its performance constraints. Therefore, designing HF modem auto generation control (AGC) circuit has become a very important design element. AGC is an important design in the shortwave transceiver, which has a very key role for improving the reception range of the receiver and overcoming the distance effect of wireless link. In the AGC circuit, although the input signal amplitude is large, the amplitude of the output signal remains constant or automatic control circuit in a small range only. The basic principle is to produce an AGC level varies with the input DC voltage AGC, AGC voltage to control the use of certain gain amplifying component, so that the total gain varies according to certain rules [2].

Currently, there are two main shortwave receiver amplifier gain control methods. One is to change the parameters of the amplifier itself, so that the gain is changed, typically dual gate FET, wherein by changing a DC bias voltage of the gate of the gain changes; the other is inserted between the amplifier stage variable attenuator to control the amount of attenuation, the gain changes, typically various integrated variable gain amplifier, AGC circuit discussed here is the United States the use of AD (Analog Devices) variable gain amplifier AD603's combination of simple AGC the control circuit to achieve. The input signal can be achieved when 100mv ~ 2500mv change, gain greater than 21dB, AGC dynamic range greater than 30dB, the output signal level basically stable at 310mv.

Chip of AD603

The AD603 is a low noise, voltage-controlled amplifier for use in RF and IF AGC systems [3]. It provides accurate, pin-selectable gains of −11 dB to +31 dB with a bandwidth of 90 MHz or +9 dB to 51+ dB with a bandwidth of 9MHz. Any intermediate gain range may be arranged using one external resistor. The input referred noise spectral density is only 1.3nV/√Hz, and power consumption is 125mW at the recommended ±5 V supplies. The decibel gain is linear in dB, accurately calibrated, and stable over temperature and supply. The gain is controlled at a high impedance (50 MΩ), low bias (200nA) differential input; the scaling is 25 mV/dB, requiring a gain control voltage of only 1 V to span the central 40 dB of the gain range. An overrange and underrange of 1 dB is provided whatever the selected range. The gain control response time is less than 1 μs for a 40 dB change.

The AD603 functional block diagram is shown in Figure 1.

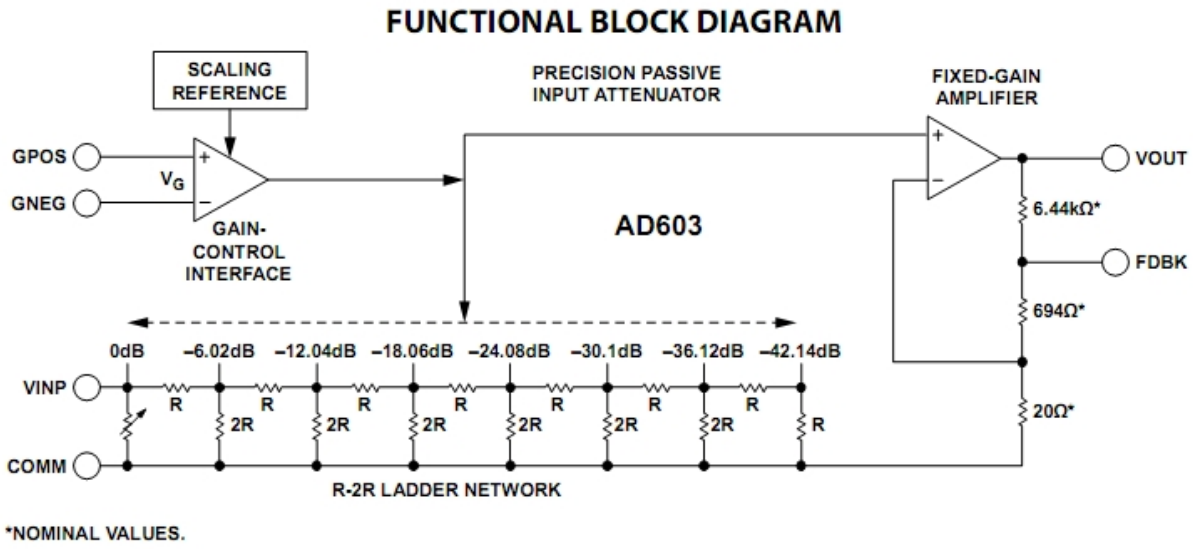

Figure 1. The Function Block Diagram of AD603

The AD603 can be used for RF / IF AGC circuit systems, video gain control, A / D range extension and signal measurement system. It provides accurate, pin-selectable gain, when 90 MHz bandwidth, gain range is -11 dB to +31 dB, gain bandwidth of 9 MHz ranges or +9 dB to +51 dB. An external resistor can be used to obtain any intermediate gain range [4].

The AD603 pin functions are shown in Table 1:

Table 1 . Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GPOS	Gain Control Input High
2	GNEG	Gain Control Input Low
3	VINP	Amplifier Input
4	COMM	Amplifier Ground
5	FDBK	Connection to Feedback Network
6	VNEG	Negative Supply Input
7	VOUT	Amplifier Output
8	VPOS	Positive Supply Input

The AD603 by the passive input attenuator, composition gain control port and a fixed gain amplifier three parts. FIG. 1 is applied to the input terminal after ladder network (VINP) signal attenuated by a fixed gain amplifier output, the amount of attenuation applied voltage is determined by the gain control interface in. Gain adjustment voltage value independent of its own, but only the difference between the VG and its related control voltage GPOS / GNEG pin input resistance up to 50MΩ, so that the input current is very small, resulting in an external circuit to affect the on-chip control circuitry provides gain control voltage decreases. It is suitable for the above characteristics constitute programmable gain amplifier. Figure 1 "slide arm" from left to right is continuously moving. When connecting VOUT pin and FDBK two are not the same, the amplifier gain range is not the same.

When the pin 5 and pin 7 shorted, AD603 gain of 40Vg + 10, then the gain range is -10dB ~ 30dB, it is designed as a basis and reference. When the foot 5 and 7 feet off, a gain of 40Vg + 30, then the gain range of 10 ~ 50dB. If at 5 feet and 7 feet connect resistors, the gain will be in the range between them.

Design of the AGC circuit

The circuit of AGC Module is shown in Figure 2 [5].

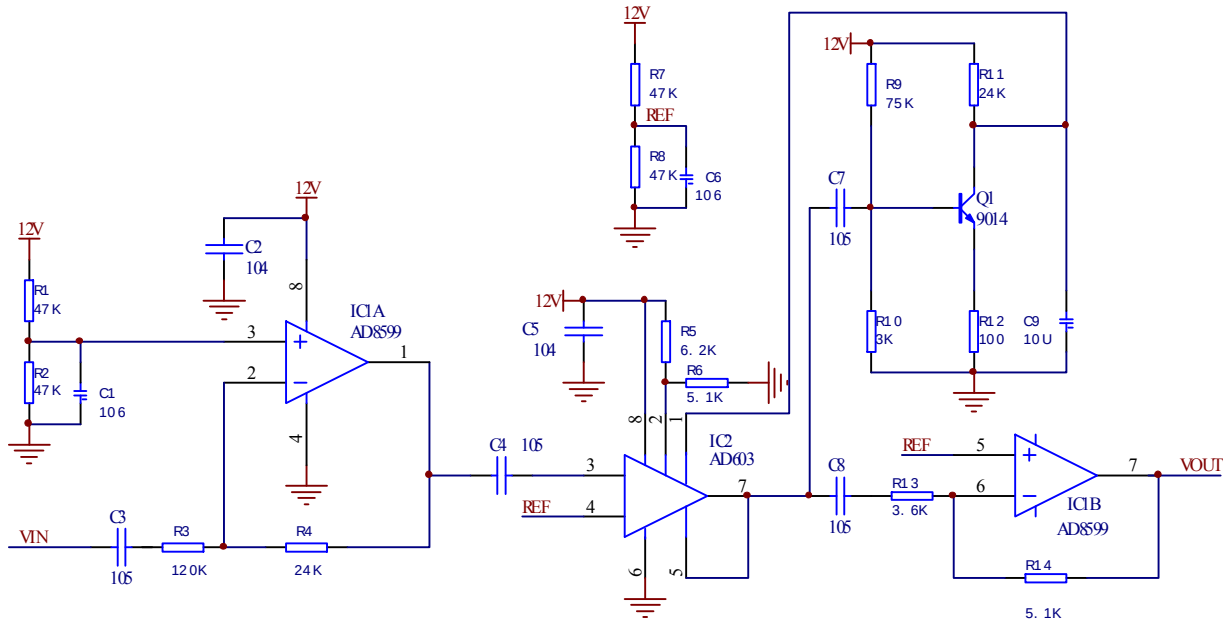

Figure 2. The circuit of AGC Module

The signal is input from pin VIN, attenuated after IC1A 3 1/5 feet added to the AD603. The signal is amplified and output two routes after AD603. One way is amplified and sent to A / D input terminal. Another way is used for AGC demodulation. The PN of Q1 finish AGC demodulation junction completed by the collector AD603 to pin 1 after filtering capacitor C9.

The voltage of pin 2 drop to the ground is fixed at 5.4V. The voltage of pin 1 drop to the ground is VAGC. Thus the voltage between pin 1 and pin 2 named V12 is controlled by VAGC. AD603 gain can be expressed as: G = 40 • V12 + 10. Thus, with the increase of VAGC, V12 will increase, and the AD603 gain increase. On the contrary, if VAGC reduced, V12 also decreased, and the AD603's gain becomes small. So that the output signal of AD603 is a constant in strength. The AGC time constant can be adjusted by varying the capacitance C9 to achieve.

When the input signal increases, the base current of Q1 instantaneous will increase. The corresponding collector current will increase. So the instantaneous voltage of R11 will increase. The collector voltage decreases instantaneously. After filtering the resulting VAGC reduces accordingly. So AD603 gain reduces. Similarly, when the input signal reduces, VAGC will increase. So the AD603 gain increases. The output signal essentially unchanged when the input signal changes.

The design requirement is that when the input signals VIN change at 100mv ~ 2500mv, the VOUT output 310mv ± 5%. After IC1A output attenuation, the amplitude at 1 foot of IC1A is 20mv ~ 500mv. IC1B is the fixed gain amplifier 1.4 times. Therefore, the output of AD603 should be 221.4mv, which determines the scope of AD603 gain in 20.8dB ~ -7.1dB. The gain of AD603 is: G = 40 * V12 + 10. The control range of V12 can be calculated in 0.27V ~ -0.43V, then the range of VAGC is in 5.67V ~ 4.97V.

From the above analysis, when the AGC control voltage changes from 5.67V to 4.97V, the total gain of AD603 changes from 20.8dB to -7.1dB linearly. It only need to adjust the operating point of Q1. Once the input signal changes, the AGC control voltage VAGC can be obtained from 5.67V to 4.97V from Q1. As can be seen from Figure 2, VAGC depend on the size of the resistance R11 and the collector current. The adjustment of the control voltage VAGC of is to rely on R9. The adjustment method is that if the input signal VIN is 100mv, according to adjusting R9, the output VOUT is 310mv.

After the completion of the circuit design, the method shown in Figure 3 can be tested [6].

Figure 3. Schematic diagram of test method

Test data can be seen in Table 2. When the input signal strength changes from 100mv to 2500mv, the AGC control circuit adjusts accordingly the size of AGC control voltage VAGC. The voltage of VAGC changes the AD603's gain, so the output signal strength basically will be stable at 310mv ± 5%, which meets to the design requirements.

Table 2. Test data of AGC

Input Signal (mv)	100	400	700	1000	1300	1600	1900	2200	2500
VAGC(V)	5.76	5.74	5.56	5.45	5.38	5.32	5.26	5.20	5.13
Output Signal (mv)	300	305	309	311	310	304	299	292	288

Conclusion

This article describes the AGC amplifier control circuit design method based on AD603. The test data has been obtained through the experiment. The result proved that the design met the design requirements. This design has been used in product development, and achieved good results.

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