

Design of Image Tracking System for Strapdown Seeker based on FPGA+DSP

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Abstract. Strapdown seeker connect the sensor fixed on the projectile, through a large field of view to ensure the effective of target detection, in order to solve the high frame rate digital image processing and target recognition tracking problem, design a kind of based on FPGA + DSP architecture is applied in the strapdown seeker image tracking scheme. The scheme adopts full digital interface, realize the Cameralink digital image data real-time acquisition, preprocessing, target tracking, character overlay, video output, etc. In view of the seeker workflow, a target tracking algorithm is designed based on feature, through digital simulation and embed implementation. Results show that the tracker can overcome the rotation and expansion of the target, complete right on target tracking, processing speed can ensure the real-time processing of target tracking in the 20 ms.

Introduction

Concise intelligent is the goal of modern war, with precise terminal guidance function is the development trend of weapon system. Loading imaging seeker is an important means that is applied in the precise terminal guidance, strapdown seekers have the characteristics of small volume, low cost and high reliability is becoming a hot spot of current research. Strapdown seeker is the core part of the image guidance weapon, its performance directly affect the guidance of missile flight control signal, precision of missile terminal guidance performance plays a key role. Strapdown seeker is suitable for applications in close small bombs on target, for the convenience of target search, in the process of ensuring flight targets at the same time don't run out of the field, strapdown imaging seeker has a larger field of view Angle. In order to adapt to the dynamic characters of projectile, the traditional resolution of 720 x 576 PAL analog video cannot meet this need, the general frame frequency imaging detector are more than 50Hz, makes the direction of the speed of the projectile flying fast on target. Thus guidance image tracking system has become critical, need it has the characteristics of large amount of data processing and fast. For the above requirements this paper designed a kind of applied in the strapdown seeker image tracking system based on FPGA + DSP architecture, is applied to a certain type of the strapdown optical imaging seeker. Through the visualization simulation validation, proved that the tracking system can overcome the rotation and expansion of the target, complete the correct and stable tracking of target, the average processing time is less than 20 ms, meet the real-time demand in engineering.

This paper discusses and introduces the image tracking system design of strapdown seeker. The workflow of imaging tracking and Semi-physical Simulation are analyzed. Some methods for reducing error are presented for imaging system. This paper is organized as follows: Section II discusses strapdown seeker principle. The image tracking system is discussed in Section III. These include the analysis of system architecture and workflow. Semi-physical Simulation analyses for the seeker are introduced in Section IV. SectionV is devoted to the conclusions.

Strapdown Seeker Principle

strapdown seeker constitution. A strapdown seeker system structure as shown in figure 1, consists of optical cabin and electronic cabin. Imaging lens, CCD and image processing module are connected

with hull solid, no inertial device, the seeker adopting carrier settlement of inertial devices, is the characteristic of strapdown seeker, is also the difficulty, the seeker unused the inertial components and framework platform has small volume, light weight, high reliability.

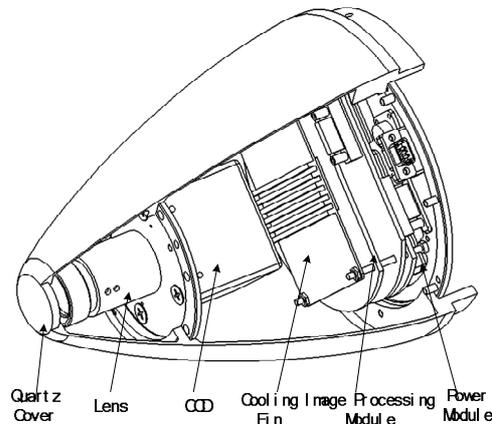


Figure 1. Strapdown seeker structure

Work Mode. The strapdown imaging seeker tracker, complete the process of missile terminal guidance, including locked automatically track targets and outputs miss distance to the onboard computer, and can be superimposed wave gate and status information on the monitor. It plays a crucial role of final hit the target. Tracker consists of three working state, capture state judgment state and tracking state, the state transition graph shown in Figure 2. When capture state, the tracker receives terrestrial wave door lock apparatus transmits the location information. Upon receiving the lock command, the system enters judgment state, through the operation if the target can be locked into the track state, if the target cannot be locked returns to capture state. When the tracking state, if received the unlock command, the system into the capture state.

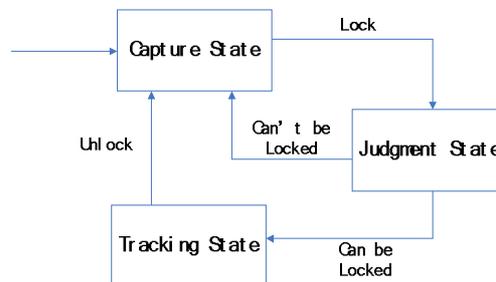


Figure 2. Work state transition graph

Image Tracking System Design

System Architecture. The system uses FPGA + DSP architecture, the use of high-speed DSP processing power and programming flexibility of FPGA design and parallel pipeline processing, to achieve the goal of real-time tracking. As shown, wherein, DSP uses TI's TMS320C6455, its clock Rate up to 1.2 GHz; FPGA uses Altera's Cyclone □ series EP3C40F484I7. System video capture, video output, serial communications, image preprocessing and OSD (On-screen display) functions are responsible by the FPGA, DSP is responsible for calculating the core algorithm. FPGA and DSP via EMIFA (external memory interface) for communication, FPGA as an external storage device by EDMA3 (enhanced direct memory access) makes data exchange between DSP.

According seeker space and size requirements, image tracking is divided into three parts, namely, power board, DSP board, FPGA board. Effect on the power supply board is to bomb power (+ 28V) is converted into seeker section camera power supply (+ 12V) and DSP board and FPGA board power supply (+ 5V). DSP board and FPGA board connected via standard high-speed board connector.

FPGA board can work independently, when the process simple task can be done independently by the FPGA to save space and cost.

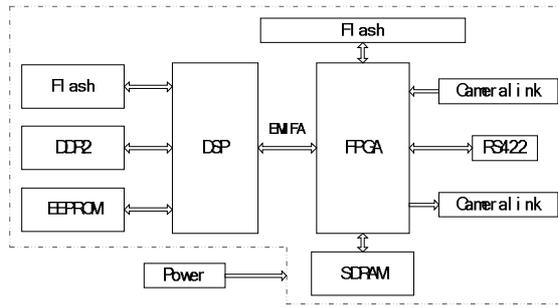


Figure 3. Image tracking hardware system architecture diagram

Workflow. FPGA board's workflow shown in Figure 4 left. Firstly the FPGA power up initialization, the digital image acquisition after initialization is complete, the receiver DS90CR286AMTD converts the 4-way LVDS data stream to 28 bit CMOS / TTL data, the maximum operating frequency can be 66MHz. 28 bit data include 24 bit image data and 4 bit image data synchronization signals consist of reserved signal, line valid, frame valid and data valid. The 28 bit data signals and a clock signal access FPGA completed image acquisition. Whether DSP startup completion signal is received, information OSD and sending a digital image display are executed. If DSP startup completion signal is received, FPGA sends the image data to the DSP board and receives some of target information from DSP board, at the same time draws window on screen.

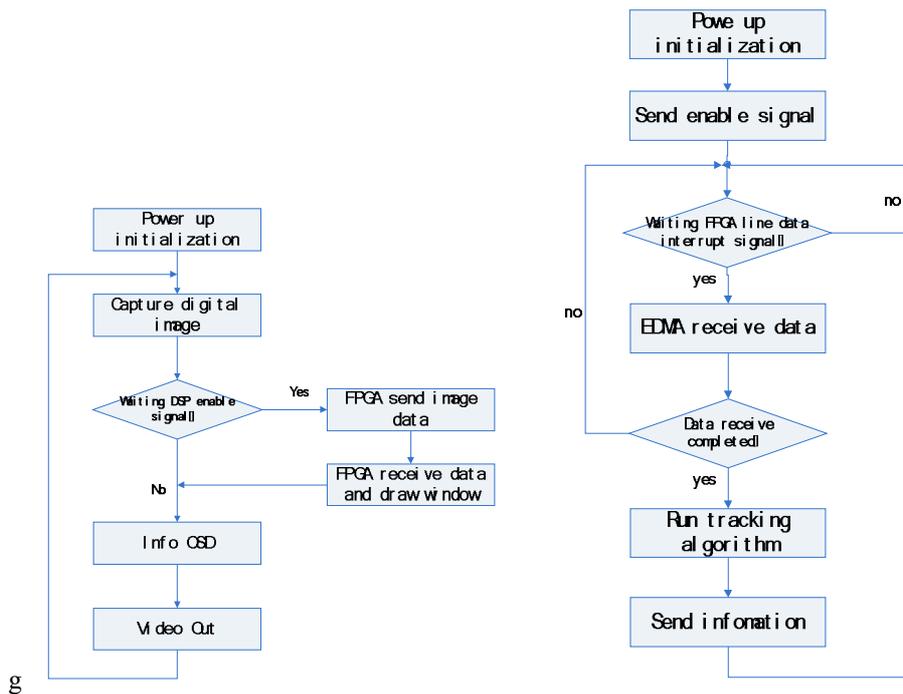


Figure 4. Strapdown seeker structure

DSP board is mainly responsible for the entire operation system tracking algorithm, the workflow shown in Figure 4 right.

Target Tracking. Image sequence having a transient continuity, when the frame rate is fast enough, the difference between the two images is very small, in a very short time frame, the moving target position change is very small, and it can be calculated to target motion by region. That image of consistency between any two adjacent image frames to find the corresponding relationship from a particular feature. The image is divided into two frames adjacent regions, each region by a similar measure to find the target. Transient continuity and consistency of the image sequence can be

expressed in the target feature similarity successive frames, and multi-frame correlation position adjacent the other aspects.

Semi-physical Simulation Analysis

Semi-physical simulation environment and conditions are shown in Table 1. Semi-physical simulation schematic diagram is shown in Figure 5.

Combat mode	lock before launch
battlefield	Mountainous environment
Missile launch height	1.5m
Missile launch posture	-3°pitch angle
distance missile project	1.2km
Target Type / Size	tank/ 2.3×2.3×5m
Camera focal length	13.5mm
FOV	± 9 ° (pitch), ± 6 ° (yaw)

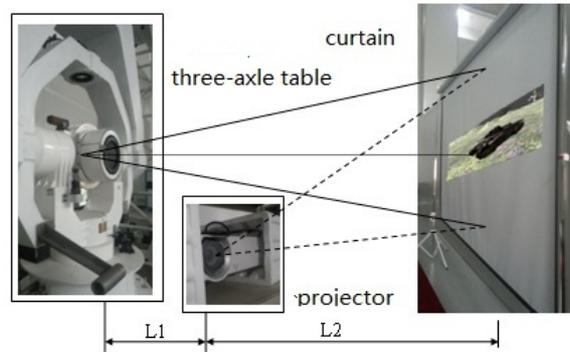


Figure 5. Semi-physical simulation schematic diagram

In the simulation experiments:

1. Artificial target identification and locking, enabling the seeker into the target tracking state.
2. Determine the projectile and target dynamics model by computer simulation projectile initial position, attitude, after the serial transfer to visual simulation machine, and projected onto the curtain to show the battlefield environment.
3. Start the flight simulation, seeker guidance system by receiving missing distance information guide and eventually destroy the target, the end of the simulation.

In the course of the entire target combat, target tracking seeker accurate, stable tracking error (before the target enters the blind spot) within ± 2 pixels.

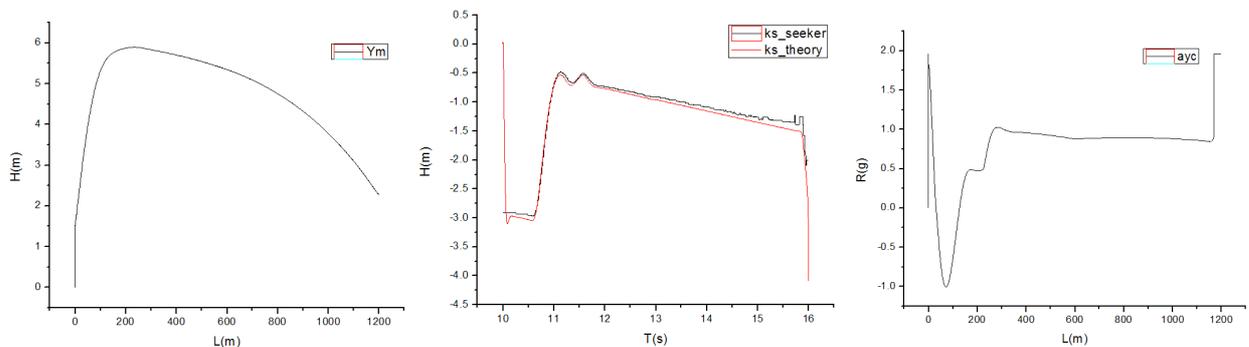


Figure 6. Strapdown seeker structure

Figure 6 left shows the longitudinal plane ballistic missile curve shown in Figure 6 middle, Seeker digital simulation and semi-physical simulation condition data comparison shows off target seeker error angle within the plane, target miss distance error is less than 0.09° and line of sight angular

velocity error value is less than $0.17\text{deg} / \text{s}$. Figure 6 right shows the overload instruction $a_{yc} \leq 2g$ to meet the needs of institutional ballistic control targets, to achieve precision strike seeker. Its average processing time is less than 20 ms.

Conclusions

In this paper, the strapdown seeker constitution and work mode are introduced. The design of image tracking system is discussed. The FPGA+DSP architecture and workflows of FPGA board and DSP board are provided. The semi-physical simulations of the strapdown image seeker are introduced. Finally, the target miss error and line of sight angular velocity error are discussed. Results show that the tracker can overcome the rotation and expansion of the target, complete right on target tracking, processing speed can ensure the real-time processing of target tracking in the 20 ms.

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