Study on the novel double-gate tunneling field-effect transistor with InAs source

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Abstract. Tunneling field effect transistor (TFET) suffers from low drive current along with severe ambipolar behavior. To resolve these bottleneck issues, a novel double gate tunneling field effect transistor with InAs source (InAsDGTFET) is proposed in this paper. By optimizing the proposed device parameters, drive current can be achieved as high as 1.09×10^{-3}A/μm, and I_{ON}/I_{OFF} ratio is 10^{10} that far more than 10^{6}. Additionally, the sub-threshold swing (SS) of 30mV/decade is gained which breakthrough the limitation of 60mV/decade that MOSFET suffers. Also, variations in source, drain and channel doping concentrations, gate work function and silicon film thickness are investigated. It is found that the device threshold voltage(V_{th}), SS, ambipolar behavior issue and drive current is more sensitive to these parameters variation.

Introduction

The scaling of conventional MOSFET is more difficult since the device size is approaching the physical limit[1]. The limit of 60 mV/decade SS at room temperature(300K) will be severe restrictions on the further development of integrated circuit(IC) and lead to an impending power crisis[2,3]. In fact, various novel devices have been investigated in recent years. And, TFET is one of the novel devices and enjoys widespread concerns. Both extensive simulations and a great deal of experimental results indicate that the SS of TFET can be well below 60mV/decade[4]-[9].

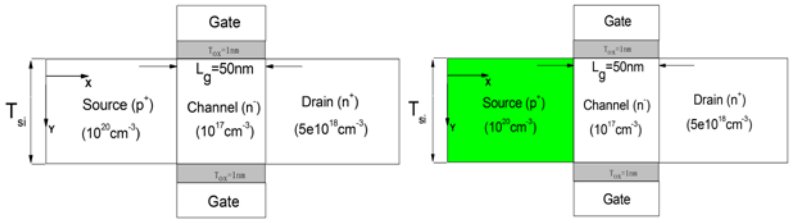
However, TFETs suffer from a low drive current and ambipoar behavior due to short channel effect(SCE)[10]-[15]. In the past few decades, a tremendous improvement in the performance of TFETs have been achieved through improved design of the device structure. Double gate(DG) architecture has been demonstrated to improve drive current[11,12]. The narrower band-gap material in source is an another effective way to improve drive current and material engineering through incorporating $Si_{1-x}Ge_x$ or InAs in source of TFET have been extensively investigated[5,16]. Ref[5] reported that drive current enhancement can be modulated by adjusting the band-gap through changing the content of Ge in $Si_{1-x}Ge_x$ material. And, some methods have been studied to solve the key issue of lattice mismatch and part of methods are applied to device fabrication[17,18]. I_{ON}/I_{OFF} ratio is an important parameter characterizing whether the device can operates in a low voltage range[19,20]. For TFET, off-state current(I_{OFF}) is defined as the current of reverse-biased leakage PN junction between source and channel region before the on-set of the tunneling current. By the same rule, on-state current(I_{ON}) is defined as the constant tunneling current after on-set until this current reaches saturation. On the other hand, TFETs exhibit ambipolar behavior, which will result in high off-state current. Three asymmetric constructions have been proposed in Ref[20] to overcome the ambipolar behavior problem. However, the device with under-lapped drain will increase the size of the device and the cost of production.

To overcome the bottlenecks of TFET and considering the feasibility of the device fabrication, we proposed a novel device named InAsDGTFET . Much higher current increases mainly depend on the enhancement of the controlling ability of the gate to channel when the Si source is replaced by a narrower band-gap material-InAs. And, the paper is organized as follows.

Organization of the Text

Devices structure and models

As presented in Fig.1, the highly doped p+ region, the lightly doped n^- region and the highly doped n^+ region serve as the source, channel and drain, respectively. Compared with the conventional DGTFET whose active region is silicon material(SiDGTFET), a narrower band gap material InAs as source region and other parameters are the same. The dimensions and doping concentrations of the devices are shown in Fig.1. Unless otherwise mentioned, gate length is 50nm, oxide thickness(T_{ox}) is 1nm with SiO_2 material, gate work function (Φ_m) is 4.35eV for gate metal and uniform doping profile type are used for these devices.



(a)SiDGTFET (b)InAsDGTFET

Fig.1 Schematic of DGTFET with Si source(a), and DGTFET with InAs source(b).

For the two different devices, source is doped p^+, drain is doped n^+, and channel is doped lightly n^-. The InAs source region is colored as green.

The simulations in this work are carried out using Silvaco ATLAS device simulator[21]. Gate leakage is overlooked in our simulations for achieving a higher drive current. V_{th} is defined as the value of V_{GS} when the drain current reaches at 10^{-7}A/μm. The physical models embodied in our simulations are listed as follows: Shockley-Read-Hall(SRH) recombination model, non-local trap assisted tunneling model, non-local BTBT model and bandgap narrowing model. Mobility model have little impact on the output characteristic in that the drive current mainly depends on tunneling characteristic. It should be noted that, the special rectangular mesh in the tunneling region should be defined carefully to make a trade-off between the requirements of accuracy and numerical efficiency. And, these meshes should be enough to include the tunneling region between source and channel region.

Results and discussion

Fig.2 shows the output characteristic at V_{GS}=1.2V and InAsDGTFET has the advantage of high drive current over SiDGTFET. The drive current of this novel device is 1.09×10^{-3}A/μm as compared with 4.26×10^{-5} A/μm for SiDGTFET.

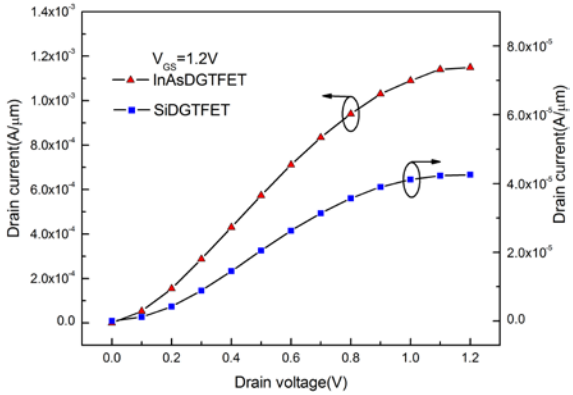


Fig.2 Output characteristic at V_{GS}=1.2V for SiDGTFET and InAsDGTFET

The expression of tunneling current is expressed [22] as:

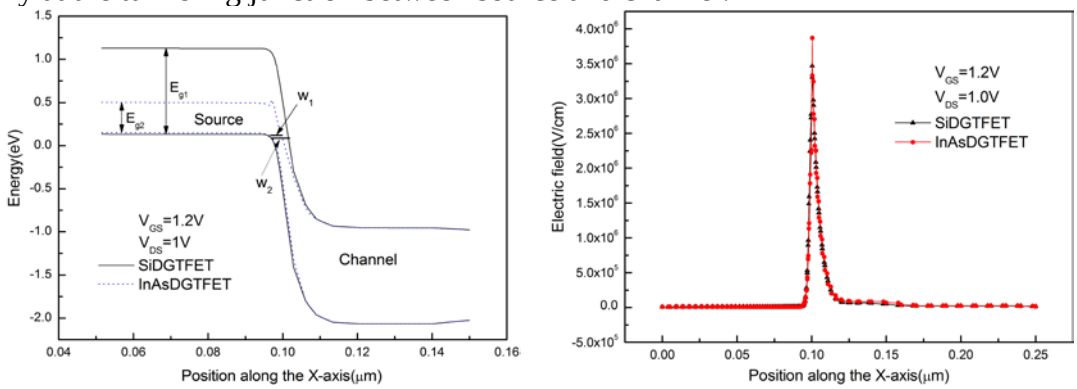
$$I_{DS} = A\frac{|E|^2}{E_g^{\frac{1}{2}}}\exp\left(-\frac{BE_g^{\frac{3}{2}}}{|E|}\right) \quad (1)$$

Where E_g is the bandgap of source region, E is the electric field, and A and B are the material-dependent parameters having default values[21] and are functions of carrier effective mass.

Thus, it is obvious in formula(1) that I_{DS} is proportional to electric field(E) and bandgap(E_g).

In order to get an insight into this phenomenon, the energy band at the distance of 1nm below the oxide-semiconductor interface is shown in Fig.3(a). When the source material is replaced by InAs, E_g narrows from Eg_1 to Eg_2, which results in reduced minimum tunneling width w_1 between the Si channel and InAs source. Respectively, w_1 and w_2 are the minimum tunneling width for InAsDGTFET and SiDGTFET.

The electric field distribution from source to drain is shown in Fig.3(b). It is evident that electric field in InAsDGTFET is larger than that in SiDGTFET. And, this is due to that hetero-junction exists between p^+ source and n^- channel in InAsDGTFET. It is apparently noticed that, the high electric field exists only at the tunneling junction between source and channel.



(a) (b)

Fig.3 (a) Simulated electron energy band for SiDGTFET and InAsDGTFET (b) Electric field distribution from source to drain, at a distance of 1nm below the interface of oxide-semiconductor for SiDGTFET and InAsDGTFET at on-state.

As depicted in Fig.4, I_{ON}/I_{OFF} ratio is found to be much better for InAsDGTFET in the entire range of gate length,as compared with SiDGTFET. And it is because of the significantly increased I_{ON} as can be observed in Fig.2.

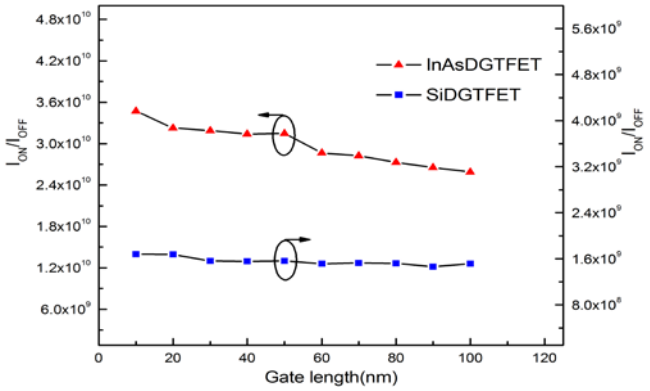
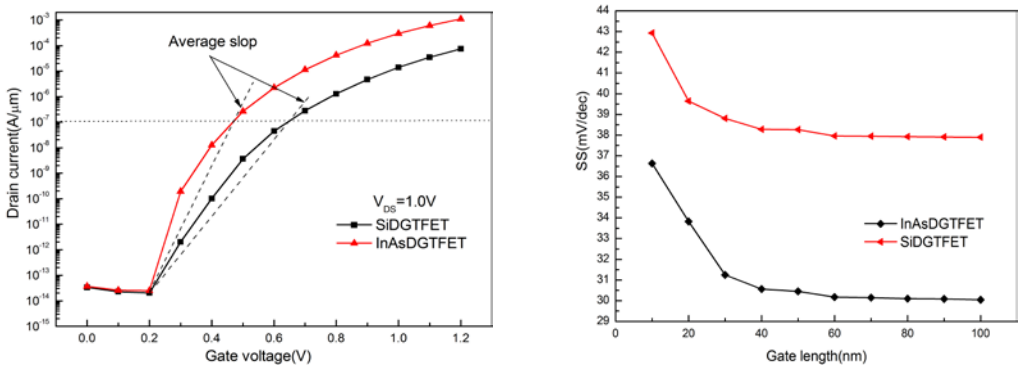


Fig.4 Variation in I_{ON}/I_{OFF} ratio(corresponding to V_{DS}=1V) with respect to gate length for InAsDGTFET and SiDGTFET.

For TFET, The average value of SS is achieved between the voltage at which drain current begins to increase quickly and the voltage when the drain current at $10^{-7}cm^{-3}$. SS can be seen relatively straightforward from the transfer characteristic curve as shown in Fig.5(a). Noted that the SS of InAsDGTFET is lowed than that of SiDGTFET. Also, a larger I_{ON}/I_{OFF} results in a lower SS [3].

The performance enhancement of SS for InAsDGTFET reaches about 23% greater than SiDGTFET. However, With the decreasing of gate length, the average SS is found to be degenerate for both these devices. This means SCE increases. Decreasing SS means the turn-on steepness increasing. Also, it means that the voltage supply is reduced without performance loss. As low as 30mV/decade is achieved which can be seen from Fig.5(b), that is to say, the proposed device will be helpful for low-power integrated circuits.



(a) (b)

Fig.5 (a)Corresponding transfer characteristic at V_{DS}=1V for SiDGTFET and InAsDGTFET (b) Presents the variation of SS as a function of gate length for different devices.

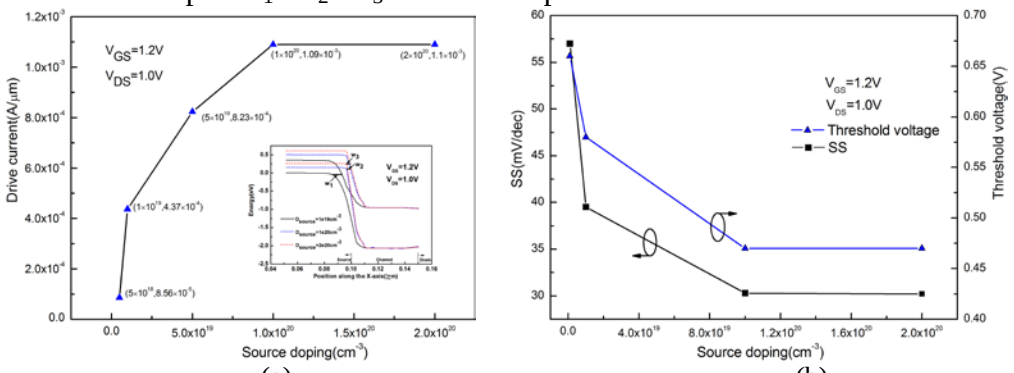
All in all, the InAsDGTFET has been shown to have some remarkable properties as compared with conventional SiDGTFET. Then, the optimization of InAsDGTFET device will be focused on to investigate the design of this device.

Optimization of InAsDGTFET device

The effects of source, drain and channel doping concentration

In this part, the impact of doping concentration on drain current and minimum off-state current will be discussed. In MOSFET, the source/drain region would be doped to be higher to restrain SCE and hot carrier reliability. For TFET, this may be different from MOSFET.

The doping concentration in drain is fixed at $5\times10^{18}cm^{-3}$. The drive current for InAsDGTFET as a function of doping concentration in source (D_{source}) is depicted in Fig.6(a). Several trends can be seen from this figure. On the one hand, as D_{source} increases, drive current increases about two orders of magnitude. However,when D_{source} is beyond $10^{20}cm^{-3}$, drive current changes a little. To understand the physics behind the relationship between drive current and D_{source}, the minimum tunneling width w can be seen from the inset figure in Fig.6(a). It is clear that w is decrease as D_{source} increase until $10^{20}cm^{-3}$ and the relationship is $w_1<w_2\approx w_3$. This corresponds to a similar increment in drive current.



(a) (b)

Fig.6 (a)Impact of source doping on drive current for InAsDGTFET (b) Impact of source doping on threshold voltage and SS.

Moreover, both SS and threshold voltage(V_{th}) is extracted at varies D_{source} as shown in Fig.6(b). This figure reveals that as D_{source} increases until $10^{20}cm^{-3}$, SS substantially improves. Meanwhile, V_{th} decreases. Therefore, D_{source} plays a dominant role to optimize the device performance for higher drive current, steeper SS and lower V_{th}.

One concern of TFETs is that they exhibit ambipolar behavior, which leads to high off-state current. The parameters remain the same as shown in Fig.1(b) except drain doping concentration(D_{drain}). The transfer characteristic is studied as shown in Fig.7. It reveals that as D_{drain} increases from $5\times10^{16}cm^{-3}$ to $5\times10^{19}cm^{-3}$, the minimum off-state current increases about two orders of magnitude and drive current increases slightly.

In order to dig out the reasons, we extract the energy band diagram at a distance of 1nm below the

interface of oxide-semiconductor, as shown in the inset figure in Fig.7. This figure is achieved in minimum off-state. No tunneling electrons could take place from drain to channel for low D_{drain}, such as $5\times10^{17}cm^{-3}$ and $5\times10^{18}cm^{-3}$. At high D_{drain}, the bottom of conduction band in drain has already lower than the top of valance band in channel and this result in a narrower tunneling width. Hence, the minimum off-state current increases. In short, D_{drain} should be modified finely to achieve a lower minimum off-state current.

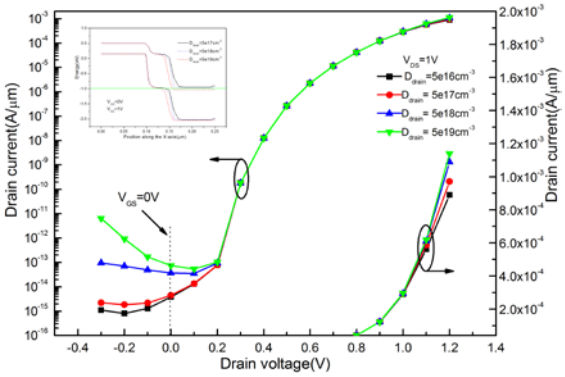
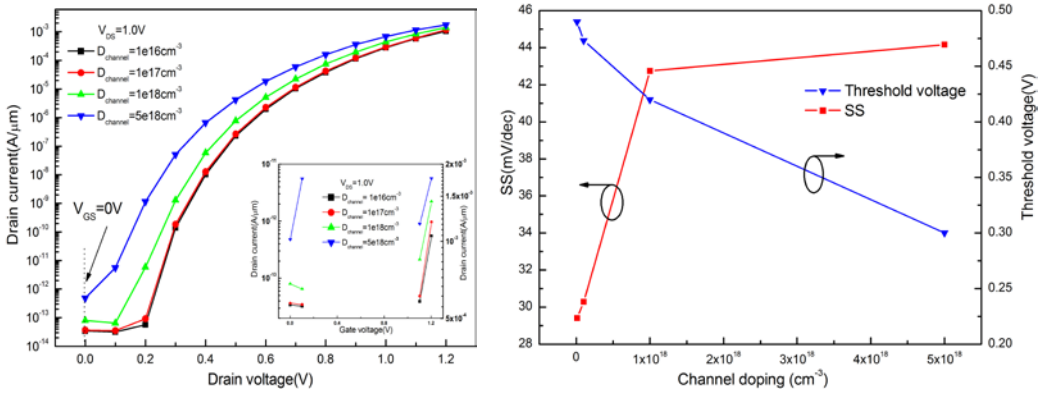


Fig.7 Device transfer characteristic for InAsDGTFET with different doping concentration in drain region. D_{drain} =5e18cm^{-3} is selected not only considering the drive current, but the minimum off-state current. Also, simulated energy band diagram at V_{GS}=0V and V_{DS}=1V across the channel at the distance of 1nm below the interface of oxide-semiconductor for InAsDGTFET with different values of D_{drain}.

Fig.8(a) shows the impact of channel doping($D_{channel}$) on the transfer characteristic of the InAsDGTFET. Drain current slightly increases as the $D_{channel}$ increases and the minimum off-state current increases at the same time. Drive current is mainly effected by the tunneling junction while minimum off-state current is always influenced by the junction between drain and channel. Drain current closely related with energy band and the energy band in channel connects both the tunneling junction and the junction between channel and drain. Therefore, both drive current and minimum off-state current can be adjusted by energy band in channel through changing $D_{channel}$. Hence, a trade-off between drive current and minimum off-state current is chosen here. When $D_{channel}$=1e17cm^{-3}, the minimum off-state current is far more small and drive current is large enough.

The impact of $D_{channel}$ on the value of SS and V_{th} are shown in Fig.8(b). It is clear that, as $D_{channel}$ increases, V_{th} decreases and SS increases at the same time. It is caused by the change in minimum off-state current and drive current which can be seen in Fig.8(a).



(a) (b)

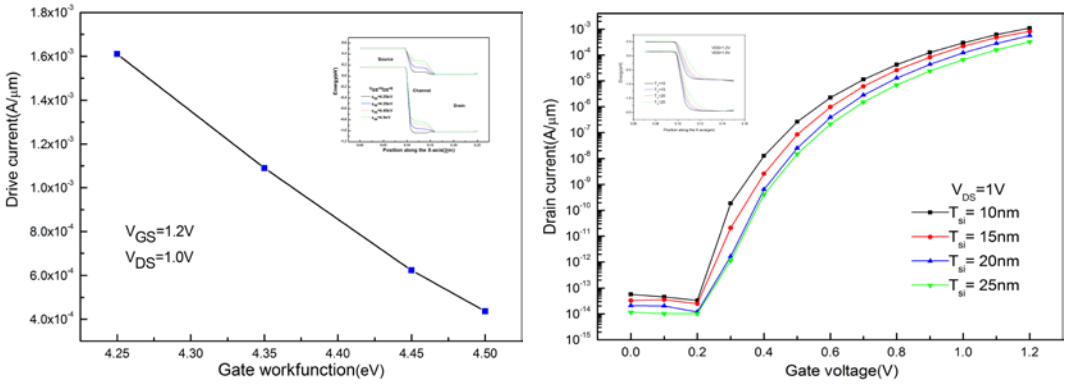
Fig.8 (a) Impact of channel doping on the transfer characteristic for InAsDGTFET (b)The impact of channel doping on SS and threshold voltage. The D_{source} , D_{drain} and $D_{channel}$ is fixed at $10^{20}cm^{-3}$, 5e18cm^{-3} and $10^{17}cm^{-3}$, respectively.

The effects of gate work function and silicon film thickness

Then, we analyze the influence of gate work function(Φ_m) on drive current for InAsDGTFET. Fig.9(a) shows the change in output characteristics as Φ_m increases from 4.25eV to 4.5eV. As expected, drive current reduces by more than one order of magnitude when Φ_m increases from

4.25eV to 4.5eV. It is caused by the changing energy band of InAsDGTFET. The inset figure in Fig.9(a) shows the change in energy band of InAsDGTFET as Φ_m increases. It can be seen that the energy band in channel become lower and lower as Φ_m decreases. The tunneling probability increases at the same time. However, when Φ_m=4.25eV, the conduction band in channel has already been lower than the valance band in source. Therefore, tunneling has been taken place in tunneling region between source and channel. Consequently, drive current begins to increase with V_{GS} increasing. This result from that the conduction band in channel could be easily pulled down until lower than the valance band by a small V_{GS}.

Fig.9(b) plots the impact of silicon film thickness on the transfer characteristic slop of InAsDGTFET. Because of the gate loses control of channel, particularly at its middle part in the vertical direction, as silicon film thickness(T_{Si}) decreases, both I_{ON} and I_{OFF} increases. It is apparently noticed that in the inset figure in Fig.9(b) that the change in energy band is more abrupt near the tunneling junction. With an increase in T_{Si}, the minimum tunneling width become larger at V_{GS}=1.2V and V_{DS}=1.0V. And, this results in an decreasing drain current. Thus, InAsDGTFET is also sensitive to T_{Si}.



(a) (b)

Fig.9 (a)The drive current for InAsDGTFET with different Φ_m. Simulated energy band diagram at V_{GS}=0V and V_{DS}=0V across the channel, at a distance of 1nm below the interface of oxide-semiconductor, for InAsDGTFET with different Φ_m. (b)Impact of T_{si} on the transfer characteristic for InAsDGTFET.Simulated energy band at V_{GS}=1.2V and V_{DS}=1V across the channel, at its middle in the vertical direction, for InAsDGTFET with variation T_{Si}.

Summary

In this work, we have investigated a novel DGTFET with InAs source to simultaneously improve the performance of the device. We demonstrate that a narrower bandgap material InAs can be applied in DGTFET to achieve great drive current, I_{ON}/I_{OFF} ratio along with the SS. Furthermore, probably impacts of structure parameters on the performance of this device are carefully studied and simulated by SILVACO simulator. After design modifications, some conclusions can be easily found out. First, a relatively higher source doping reduces the minimum tunneling width and helps us to achieve a higher drive current , a steeper SS and a lower threshold voltage. Second, as drain doping increases, the tunneling barrier distance between drain and channel increases. And this regulation will be beneficial to address the ambipolar problem. Third, not only the minimum off-state current, but the drive current can be adjusted by the channel doping. Fourth, Φ_m have a great influence on the device performance. A reduced gate work function increases the drive current. However, gate work function should not be reduced without limitation. If it is too low, tunneling will take place without V_{GS} applied. Last, Tsi can also be influenced I_{ON}, I_{OFF}. However, the solutions to address the short channel effect of device worth further explored, although there is an appreciable improvement in overall device performances.

Acknowledgments

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