Design of Synchro-to-Digital Converter Based on Digital Servo System

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***Abstract*—Structure and principle of high accuracy measurement of angle synchro/digital converter circuit are introduced based on digital servo system. The converter consists of electronic Scott transformer, D/A multiplier, phase sensitive detector, integrate, ROM, logic processor and communication interface unit. Analyzed the sine or cosine multipliers how to multiplying digital to analog converters which incorporate sine or cosine laws. The testing result shows that the applied scheme can satisfy the converter accuracy, the circuit is simple in form, and the reliability of designed system is proved in application.**

Keywords-synchro ;digital converter; data transmission

I. INTRODUCTION

Measurement of azimuth is an important technology for radars, navigation systems and control systems to supervise their states. Research and development of measurement system of azimuth becomes an important subject. Synchro is a kind of transducer, resembling micro controlled electric motors, which transmits electrical signals proportional to its shaft angle. It is widely used in navigation, industry and military equipments, and it can not only measure the angular position of remote mechanical devices, but also control the displacement of remote equipments. The synchro/digital converter has been specifically designed for motor position control for the numerically controlled machine and robot industry, using the 2 servo loop tracking principle that ideally suits these converters to the electrically noisy environment found in these industrial applications. The output word is in three-state digital logic form with a high and low bytes enable input so that the converter can communicate with an 8-or-16-bit digital highway. The synchro-to-digital conversion Used analog to digital conversion together with digital Sine and Cosine look-up tables in tradition is dependent on the absolute magnitudes of the signal input, but the tracking converter on the ratio between the signals. This method is more complicated and less accurate than the Sine and Cosine multiplier method using in the tracking converters. Because the signal in a tracking converter is integrated, the synchro/digital converter provides a high degree of noise immunity. This paper presents the principle of operation and realization of the Sine and Cosine multiplier.

II. PRINCIPLES OF OPERATION

The functional block diagram of sycho/digital converter circuit is shown in Fig.1. The converter consists of Scott T, digital sin/cos multiplier, error AMP, phase sensitive detector, integrator, VCO, and up-down counter. The converter operates on a type 2 tracking servo loop. The output digital word continually tracks the position of the synchro shaft without the need for external convert commands and wait states. As the transducer moves through a position equivalent to the least significant bit weighting, the output digital word is updated by one LSB. Assume that the state of the synchro is at angle θ, the

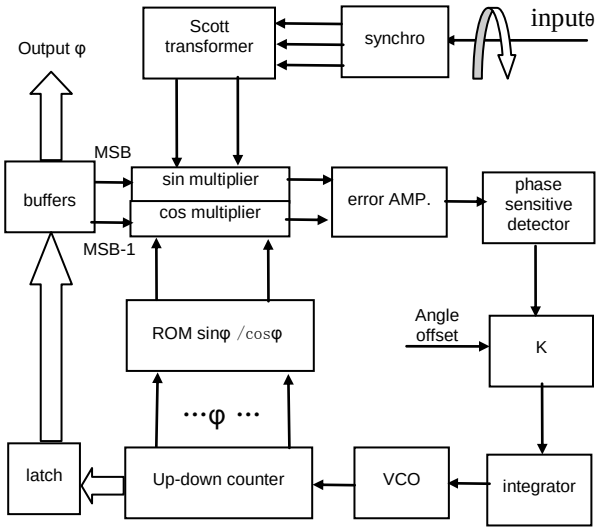

Fig.1. Synhro-to-digital converter functional diagram

system reference UR should be connected to R1 and R2 in Fig.2, when

$$U_R = U_m \sin(2\pi ft) \tag{1}$$

Then the 3 wires synchro output will be

$$U_{S_1} = KU_m \sin(2\pi ft)\sin(\theta) \tag{2}$$

$$U_{S_2} = KU_m \sin(2\pi ft)\sin(\theta + 2\pi/3) \tag{3}$$

$$U_{S_3} = KU_m \sin(2\pi ft)\sin(\theta - 2\pi/3) \tag{4}$$

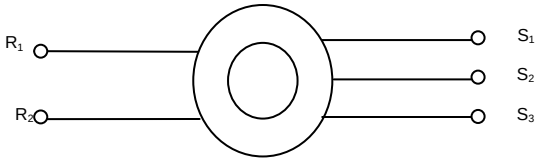

Fig.2. Sketch diagram for synchro

Electronic Scott transformer to perform a synchro to resolver format conversion is shown in Fig.3. When $R_2 = \sqrt{3}R_1$

$$U_1 = KU_m \sin(2\pi ft)\sin(\theta) \quad (5)$$

$$U_1 = KU_m \sin(2\pi ft)\cos(\theta) \quad (6)$$

The digital angle φ (i.e. the current word state of up-down counter) is applied to the sine/cosine multiplied by U_1 and U_2 to give

$$KU_m \sin(2\pi ft)\sin(\theta)\cos(\phi) \quad (7)$$

$$KU_m \sin(2\pi ft)\cos(\theta)\sin(\phi) \quad (8)$$

These signals are subtracted by the error amplifier to give the error signal that is:

$$KU_m \sin(2\pi ft)\sin(\theta - \phi) \quad (9)$$

This error signal is then fed into integrator, the output of which drives voltage control oscillator. The VCO outputs to pulses to the up-down counter until sin(θ－φ)=0 at this point θ－φ=0 or θ=φ. Therefore the internal loop will null with the up-down counter and hence the digital output representing angle θ. When this is accomplished, the word state of the up-down counter φ equals to the synchro shaft angle θ within the rated accuracy of the converter. If the input is not changing, the converter is null and doing nothing. If the input is changing, the output word automatically updates every time that the input increments through an angle equivalent to the weight of the least significant bit.

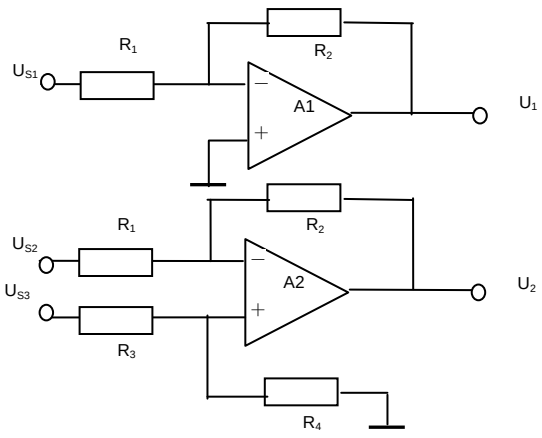

Fig.3. Electronic Scott transformer

A. The sin/cosine multipliers

The purpose of the sin/cosine multiplier is to generate an error signal. A read-only memory has the values of sinφ or cosφ stored in it for 0 ºφ≤90 º, digital angle φ is from 3rd bit and LSB digital output of up-down digital counters. Segment switching consist of digital or analogy switches D4053 used

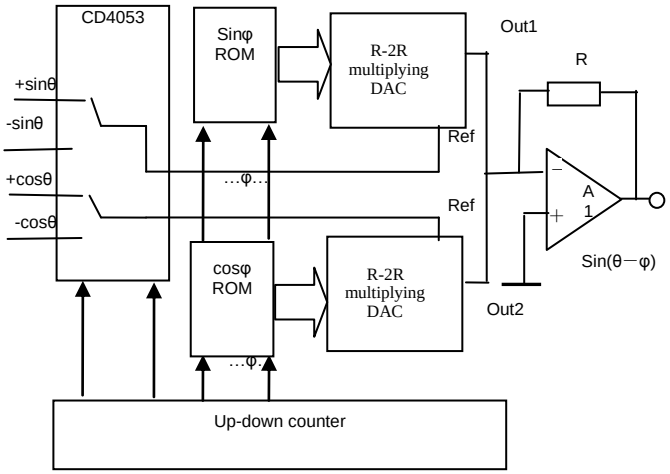

Fig.4. Sin/cosine multiplier function

to accomplish full four- quadrant multiplier. Fig. 4. shows two multiplying R-2R D/A converters used as digitally controlled attenuators multiplying the reference signals sinφ and cosφ by the vector components of φ. Using the actual resolver line voltages sinθ and cosθ as the converter reference inputs, and multiplying by digital equivalents to sinφ and cosφ, an output proportional to the angular error (θ －φ) is developed.

B. Using a tracking converter

The validity of the output data is indicated by the state of the "BUSH" output. When the input to the converter is changing, due to a change in displacement of the converter the signal appearing on the converter's BUSH output pin is a series of pulses of TTL level. A BUSH pulse is initiated each time the input moves by the equivalent of an LSB and the internal up-down counter is incremented or decremented. With the INHIBIT input pin in the "Hi" state, data will be transferred automatically to the output latches. The methods of transferring the output data is to detect the state of the "BUSH" which is "Hi" for ≥1μs and then transfer the data when the BUSH is "Lo" and the INHIBIT is "Hi" and presented to the output. The sychro/digital converter is not particularly susceptible to harmonic distortion on the signal and the reference and can be operated on square wave or triangular wave references provide that this is acceptable to the synchro.

By the control signal time series analysis, if the use of DSP to read SDC 14-bit number of output data, first of all to make all SDC's INHIBIT into a low level, and then wait to 600 ns, again make to read SDC's ENABLE signal into a low level, wait 110 ns to read the output data, For instruction cycle only dozens of ns of DSP, this will waste a lot of machine cycle, this is more serious in the case of multi-channel. To solve the problem between SDC and DSP used 4 D flip-flop and three state latch for 16 bit to implement the logic timing design between them. When the BUSY signal changes from high to low or from low to high at the moment, the latch contents will change, then read it may get the wrong data. Here let the BUSY signal delay output by D flip-flop, it can avoid the error above. Also can at the same time using multiple series D flip-flop, and cooperate with the clock signal CLK obtain appropriate blocking signal pulse width. DSP output signal INHI for high level, it didn't read the data, for the low level SDC DSP is read data, When the DSP does not need to read data, INHI is set to a high level, BUSY falling edge of each pulse triggers a latch, so it can be transformed every angle to each latch latches, When DSP needs to read data from each channel, first INHI is set to low level, thus prohibiting a change in the content of the latch, and then through the output enable end to read each latch data, without any wait states, greatly improving the real-time control system, only after reading INHI is set to a high level.

C. The main specification

Accuracy	±8.5'
Resolution	12bit(Natural Binary)
Signal Voltage	11.8Vrms~90Vrms
Signal Frequency	400Hz
Frequency Voltage	26Vrms~115Vrms
Load	8TTL
Logic Levels	TTL/CMOS
Tracking Rate	2400rpm
Power Supplies	±12V
Power Dissipation	1W
Temperature	0℃~＋70℃
Weight	≤30g
Bit Weight	SEE TABLE I

TABLE I. BIT WEIGHT

Binary	Degrees	Binary	Degrees
1	180.0	7	2.8125
2	90.0	8	1.40625
3	45.0	9	0.703125
4	22.5	10	0.351562
5	11.25	11	0.17578125
6	5.625	12	0.087890625

III. CONCLUSION

The synchro has been known for many years as an accurate method of controlling machine tools and other control system. Tracking synchro to digital converters can be considered functionally identical to resolver to digital converters, and in fact converters type in principle can be used with both inductosyn and resolver .In a typical central computer-based position-control system where a synchro and SDC constitute the primary feedback elements, the SDC produces a 12-bit digital word proportional to the inductosyn slider's position within one pitch of the scale. The SDC's output also includes direction signal, and a ripple-clock signal, which indicates when the scale moves from one cyclic pitch to the next. A similar circuit configuration can be used in application where a resolver and converter are used with a lead screw. Take the synchro wwaveform as the transformation goal, has designed the digital/synchro converter, and has given the corresponding error test method. If applies it in the digital/ resolver form signal production, only need remove the Scott transformer, and changes the reference voltage amplifying circuit's enlargement factor to adapt resolver transformer's voltage and the power requirements.

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