A Novel Clock circuit used in Time-Interleaved ADC

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Abstract. This paper presents a new type of clock system based on standard CMOS 0.18μm, 1.8V process. It can be used for 14bit, 500 MHz sampling frequency, time interleaving (TI) ADC. The clock edge reassignment technique has been introduced in this paper. Simulation has been run in Spectre under Cadence platform. The result shows that this clock circuit is especially useful in a 14bit, 500MHz sampling frequency high speed TI ADC and the timing mismatch is less than roughly 2ps , which meets the design requirement.

Introduction

High-performance analog-to-digital is a common key technology to support the new generation broadband wireless communication system. With the rapid development of digital technology, high-speed high-precision analog-to-digital converter (ADC) becomes the technical bottleneck of the system application. However, with in present technology, ADC's performance is approaching limitation after years of research. When a single ADC has reached the limits of existing design and process conditions, in order to break the constraint of conversion rate, the parallelization method is a good choice. With each channel ADC (Sub-ADCs) sampling the input alternately, this ADC implementation is called time interleaving structure. However, offset mismatch, gain mismatch, and timing mismatch among channels seriously deteriorate the performance of time-interleaved ADC. Three kinds of mismatch can be eliminated by correction, but the bigger the mismatch, the greater the difficulty of design correction method, especially for dealing with timing mismatch, existing methods can not improve performance substantially, or the method are very complicated. Therefore, in the design of clock system for TI-ADC, the timing mismatch between the two channels needs to be as small as possible.

The timing mismatches influence on TI-ADC parameters

In an ideal situation, double channel time interleaved ADC uniformly alternate sampling, the sampling clock interval of adjacent channel are T. But in the actual time interleaved ADC, there exist timing mismatch, its value is ΔT. Because of the existence of timing mismatch, the sampling time of even channel A is lagging behind in ΔT/2, and the sampling time of odd channel B is ahead ΔT/2.

If the input signal is $\cos(wt + f)$, then the quantitative result for TI-ADC is:

$$y[n] = \cos[wT + \Delta T / 2) + f] \tag{1}$$

In the Eq.1, N is even.

$$y[n] = \cos[wT - \Delta T / 2) + f] \tag{2}$$

In the Eq.2, N is odd.

The samping time is unified for $nT + (-1)^n \Delta T / 2$, so,the above two expressions can be merged into one equation:

$$y[n] = \cos\{w[nT + \frac{(-)^n}{2} \Delta T] + f\} \tag{3}$$

According to the triangle change, Eq.3 can be the following equation:

$$y[n] = \cos(\frac{w\Delta T}{2})\cos(wnT + f) + \sin(\frac{w\Delta T}{2})\sin[(w - \frac{w_s}{2}nT + f] \quad (4)$$

Among them, w_s is the clock sampling frequency . The fist of the expression is the ideal sample amplitude that is slightly reduced because of the sampling time deviation of ΔT. At the same time,the second of the expression is distortion, the amplitude is $\sin(w\Delta T / 2)$, and the frequency is $\left|w - \frac{w_s}{2}\right|$.

So, the relative amplitude is :

$$\frac{\sin(w\Delta T / 2)}{\cos(w\Delta T / 2)} = \tan(w\Delta T / 2) \approx \frac{w\Delta T}{2} \quad (5)$$

At a certain input frequency, the timing mismatch between the channels determines the relative amplitude.The smaller the timing mismatch, then the higher the linearity of TI-ADC.

The traditional architecture

As shown in Fig.1, in the dual channels time interleaved ADC, two interleaved samplers SHA1 and SHA2 require two corresponding clocks CK1 and CK2, which are typically generated by a frequency divider.

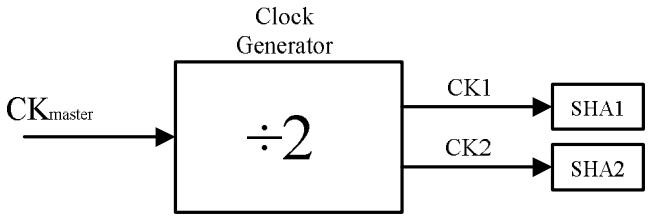

Fig.1 Block diagram of the traditional clock circuit

Two frequency dividers are generally composed of D flip-flop, the D flip-flop structure is shown in Fig.2, and here is how it works: The Φ1 and Φ2 are the two-phase no overlapping time series. When Φ1 is high level and Φ2 is low level, the input is connected to the master latch, and disconnected from the slave latch. Hence, the output Q remains the logical value of the previous stored in the slave latch, and the loop of the slave latch is closing. The node capacitor of the master latch will be charged, forming the charge of the voltage equivalent to the current voltage at the input D. when Φ1 is low level, the master latch is disconnected from the data input. Then, when Φ2 is high level, the feedback loop of the master latch is closing, and lock on the value of D. Simultaneously, the output is connected to the slaver latch; its feedback loop is opening. The node capacitor of the slave latch will be charged, hence, when Φ1 becomes high level, the slave latch is locked in a new logical value, and output Q=D.

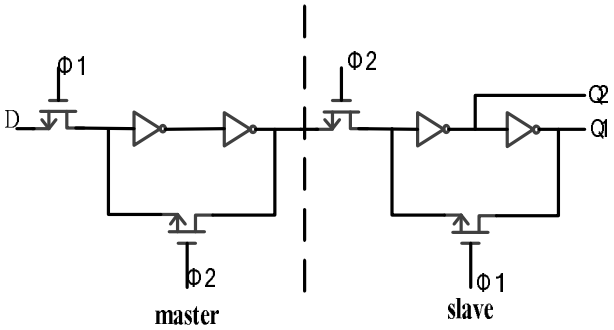

Fig.2 Master-slave D flip-flop

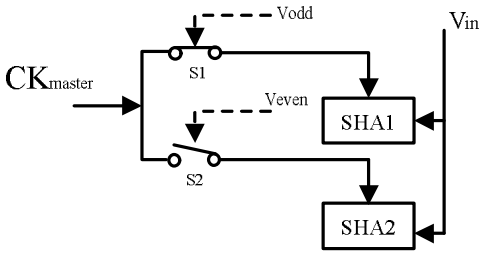

Fig.3 Block diagram of the novel clock circuit

This clock system is simple , but there is a big shortcoming. On the circuit diagram, the output of the frequency divider is not completely symmetrical. As show in Fig.2 , the output of inverter Q3 is CK1, but the output of Q3 needs to go through another inverter, its output is CK2. In the design process, To match the CK2, we can get the CK1 to pass a transmission gate , but this natural asymmetry is certainly not entirely matched. Therefore, CK1 and CK2 will have inherent timing mismatch. When the master

clock frequency is 500MHz,the timing mismatches between CK1 and CK2 will exceed 8ps, such a timing mismatches will greatly increase the design difficulty of the correction unit.

The proposed architecture

In order to reduce the design difficulty of the correction unit in ADC, especially the correction unit of timing mismatch. We should make the timing mismatch between two channels as small as possible in the design of TI-ADC. Because the traditional clock system can't meet this requirement, we design a novel clock system, as show in Fig.3. Among them, CK_{master} is the master clock, SHA1 is the sample and hold unit in odd channel, SHA2 is the sample and hold unit in even channel. V_{odd} and V_{even} are slave clock , its frequency is half of the master clock. The master clock is connected to the S/H of the single channel through the selective switches S1 and S2.

V_{odd} and V_{even} are very coarse,which are generated by a frequency divider through the master clock. they do not have the duty cycle and jitter requirements. Just ,it is assures that the falling edge of the master clock can fall at the high level of the clock.

The design of switches S1 and S2 is key, we cannot simply use the transmission gate or the three state selector to make the switches. Specific circuit is shown in Fig.4. The time sequence of the master clock and slave clock are shown in Fig.5. The master clock CK_{master} produces the clock CK_{1X} and CK_{2X} through different inverter. Their frequency is the same,the phase is the opposite. As the time sequence can be known, the falling edge of the master clock CK_{master} will be situated in the high level of the slave clock ,and the falling edge will be situated in the low level of the slave clock. In addition, the high level of the V_{odd} and V_{even} is not overlapped. Hence, when the V_{odd} is high level, the V_{even} is low level, PMOS M2 and NMOS M3 are opening, PMOS M1 and NMOS M4 are closing, the first falling edge of the master clock produces the rising edge of the CK1 and the falling edge of the CK2; when the V_{odd} is low level, the Veven is high level, PMOS M1 and NMOS M4 are opening, PMOS M2 and NMOS M3 are closing, the second falling edge of the master clock produces the rising edge of the CK2 and the falling edge of the CK1.

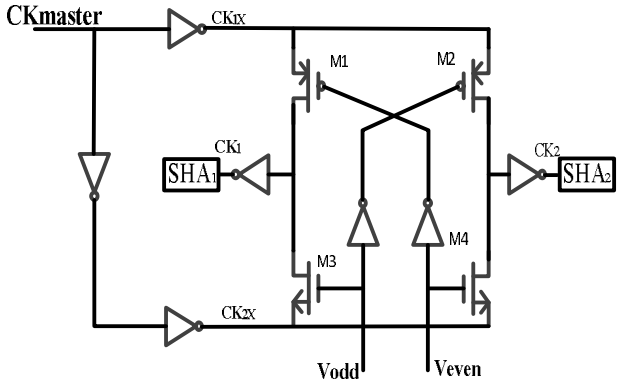

Fig.4 Novel clock circuit

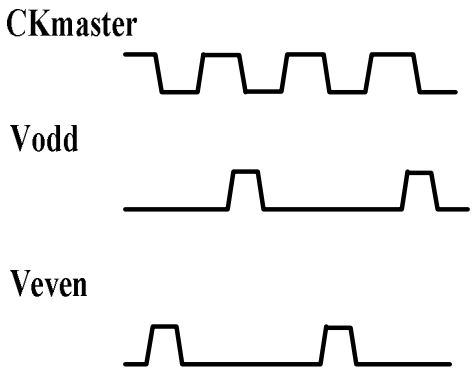

Fig.5 The time sequence of clock

In reality, each SHA requires both a rising edge and a falling edge to perform the sample and hold operations. the falling edge of CK_{1X} and the rising edge of CK_{2X} are alternately applied to the SHA's, while the rising edge of CK_{1X} and the falling edge of CK_{2X} are discarded. The actual sequence of operation is as follows. First, the falling edge of CK_{1X} is routed to SHA1 and the rising edge of CK_{2X} to SHA2. Next, the states of CK1 and CK2 are stored. Subsequently, the falling edge of CK_{1X} is rerouted to SHA2 and the rising edge of CK_{2X} to SHA1. This concept can be easily extended from two channels to three or more channels. The front-end sample-and-hold circuit used in this work incorporates three channels.

As a result, the double edges of the CK1 and CK2 are generated by the master clock edge reassignment, the timing mismatch is now equal to the delay mismatch of the falling edge of the master clock . Hence,the timing mismatch between the channels of this TI-ADC is reduced greatly , In the 500MHz sampling frequency, the timing mismatch is less than roughly 2ps between the two channels.

Simulation

The proposed clock circuit is designed in a 0.18um standard CMOS technology with a 1.8v supply. Simulation has been run in Spectre under Cadence platform. The input signal is a sine wave of 10MHz, and the frequency of sampling signal is 500MHz. Simulation of TI-ADC using the traditional clock circuit and using the novel clock circuit. The results are shown in Fig.6 and Fig.7. The spurious power is -72dB ,which is introduced by the timing mismatch in the TI-ADC using the traditional clock circuit. and the spurious power is -81dB in the TI-ADC using the novel clock circuit.

The simulation results show that the novel clock circuit can reduce the timing mismatch between the channels in the TI-ADC.

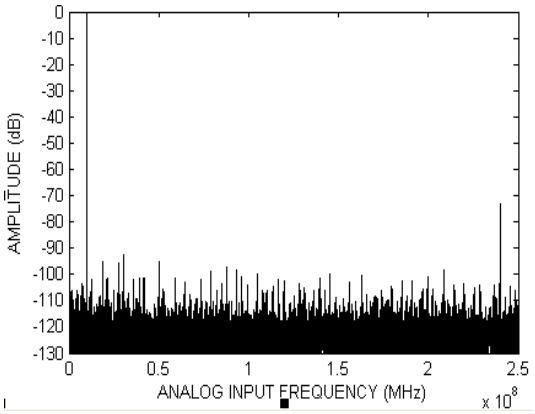

Fig.6 The output spectrum of the TI-ADC with traditional clock circuit

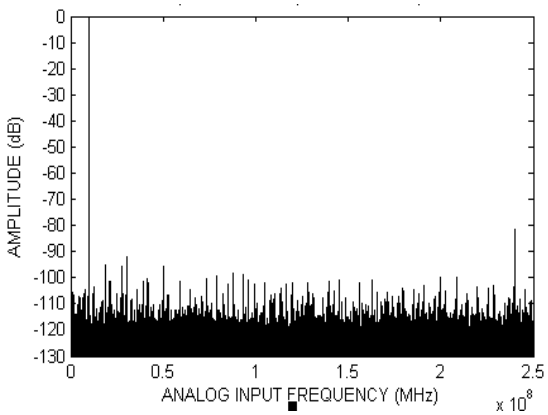

Fig.7 The output spectrum of the TI-ADC with novel clock circuit

Conclusion

For the TI-ADC, the timing mismatch between channels will generate a distortion at the frequency of $F_s/2-F_{in}$. The amplitude of the distortion is determined by the amount of mismatch. In order to lower timing mismatch, we employed a new technique that is the clock edge reassignment. This novel clock circuit converts the timing mismatch between the two channels to the delay time between the falling edge of the master clock. The timing mismatch between the channels of the TI-ADC is reduced greatly.

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