A 1.8V 12-bit 1GS/s SiGe BiCMOS time-interleaved Analog-to-Digital converter

Mingyuan Xu[1,a*], Liang Li[1], Xiaofeng Shen[1],Xi Chen[1]

[1]Science and Technology on Analog Integrated Circuit Laboratory, Chongqing, China,

[a]xmymars@163.com

Keywords: pipelined ADC, time-interleaved, recode Calibration

Abstract. This paper describes a 1.8V 12 bit 1 GS/s pipeline ADC realized in a 0.18 μm BiCMOS SiGe process. The ADC consists of a two-way time-interleaved hierarchical structure. Each sub-ADC consists of one input buffer and T&H with BiCMOS technology which improves the dynamic performance and reduces the converter error rate. The interleaving spurs caused by channel mismatch use OTPNVM to recode calibration. It achieves an SFDR of 87dB at 200MHz. Spectre simulation shows that the spurs of the channel mismatch achieve less than -106dB at gain and timing error, -97dB at the offset error.

Introduction

High-precision and high-speed analog-to-digital converters with a single core achieving high conversion rate are very difficult to realize. So multiple-core architectures with time-interleaved can be used to increase sample rates [1]. But the capability of digitizing signals with bandwidths needs to accord with the sample rates. Test instruments, such as wideband digitizing oscilloscopes, continually demand A/D converters with increased sampling rates and greater input bandwidth. Although the time interleaving of many parallel electronic A/D converters can enable very high aggregate conversion rates, the effective resolution of the converter at high input frequencies remains limited by the bandwidth and aperture jitter of the input sample-and-hold circuit.

This paper introduces a two-way A/D converter, the architecture using SiGe BiCOMS input buffer circuit which can achieve 1GHz full power bandwidth (FPBW). The error of two channels can be calibrated the One-time programmable non-volatile memory (OTPNVM) which fused the calibration information of the offset, gain and timing error correction [2]. Pipelined ADCs designed in analog BiCMOS technologies can offer good linearity and high SNR performance for input signals with reasonable voltage swings. Such ADCs, however, face two critical design challenges: the mismatch of the two-way limits the performance, the FPBW limits the analog input frequency. This paper introduces a time-interleaved (TI) 1Gs/s 12b pipelined ADC in SiGe BiCMOS that addresses these issues.

The Architecture

Fig.1 shows the block diagram of the 12-bit 1Gsamples ADC. It consists of two 12-bit 500Msps ADCs. During operation, the clock block selects each way in turn to process the analog input signal. The corresponding digital multiplexer selects the digital output of the selected way and forms an effectively 1G samples ADC.

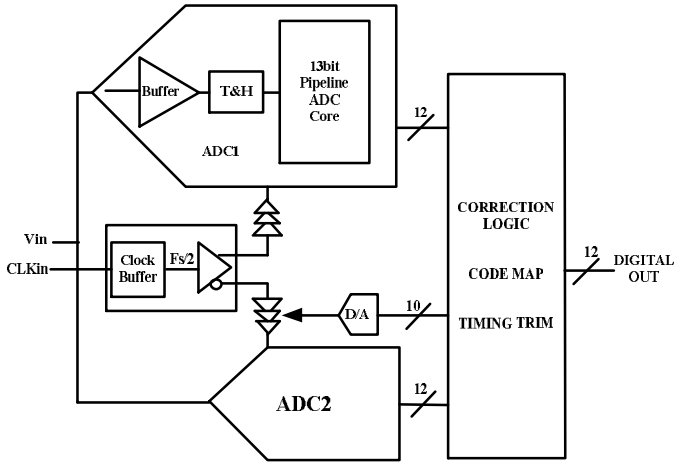

Fig.1. Top level two-way TI ADC architecture

Each channel in the ADC consists of one input buffer, one T/H and eight pipelined stages. The input buffer which achieves 1G FPBW is shown in Fig.2. The buffer alleviates the input loading problem. The input is terminated by a 50Ω resistor to a common mode (CM) voltage and drives three emitter-follower (EF) buffers. The first EF buffer drives the sampling switches of the T/H, the second EF buffer drives the bootstrap circuits to isolate them from the signal path and the third EF buffer drives the comparator of first stage. The low output impedance of the EF drives the top-plate sampling switch and achieves high SFDR. A resistor between sampling switch and the sampling capacitor improves the linearity of the switch.

The channel mismatch is recorded by the OTPNVM. Timing skew is adjusted using a 10b DAC to supply the clock buffer power supply which can change input-clock propagation delay.

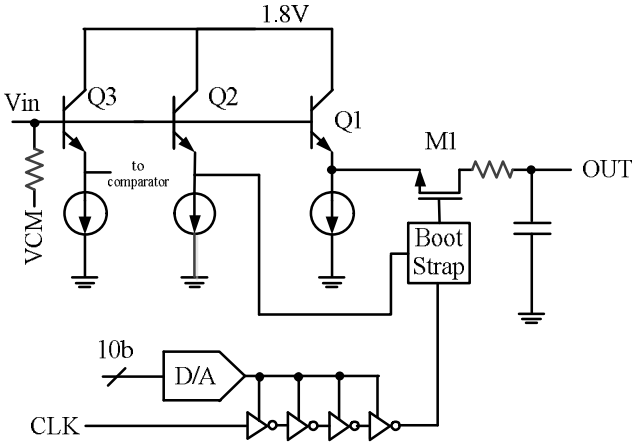

Fig.2. Input buffer and track/hold

Channel Mismatch Correction

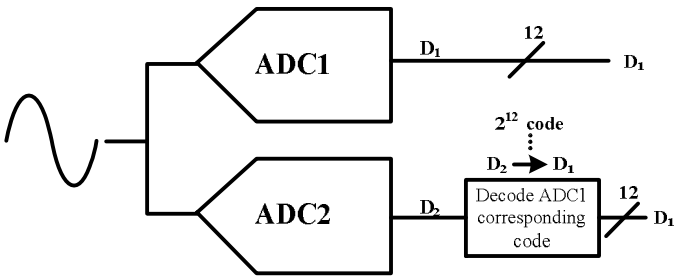

Fig.3. Block diagram of the ADC calibration

Based on the large capacitance of OTPNVM, all the calibration codes can be well recorded. So in this paper we present an off-chip method which can probing mismatch of channels, and use OTPNVM to fuse the correction information. The channel offset and gain error calibration flow is shown in Fig.3. When two channels ADC sampling the same analog voltage, the ADC1 convert this voltage to 12bits

bin D1, and the ADC2 convert the same voltage to 12bits bin D2. Digital codes D2 will be decoded ADC1 corresponding code such as D1. In this case ADC1 and ADC2 have the same codes outputs of the same analog input voltage. As a result, the offset and the gain mismatch errors of the channels are corrected.

The table of the codes which ADC2 look up must be tested off-chip. In the test mode, two channels has the same analog input, recode each converted codes and, and at the sample point find the full codes one by one. Finally use OTPNVM to fuse the map table of the new codes.

The timing mismatch of the two channels also uses off-chip testing to calibration, high-frequency test signals are required and the detection of timing differences requires sophisticated algorithms. The effect of timing skew increases with input frequency. A statistical bound on the acceptable skew with a sinusoidal input [3] for a given target resolution is Eq.1.

$$s_t^2 = \left(\frac{N}{N-1}\right)\left(\frac{2}{3 \cdot 2^{2B}(2pf)^2}\right) \quad (1)$$

Which is a function of the interleaving factor, input frequency f, and target resolution. This bound is relaxed when wideband signals are analyzed. In the case of a two-way interleaved ADC as in this paper, a deterministic relationship between the skew-related SFDR and timing skew is easily derived for sinusoidal input signals as Eq.2.

$$SFDR_{dB} = 20\log_{10}(\cot(pft)) \quad (2)$$

In this design, we target approximately 100 fs of timing skew. Symmetric layout removes systematic mismatches [4], with residual routing and transistor variations limiting timing-skew related performance. For this reason, calibration techniques are implemented in this design such that the timing skew can be corrected.

Simulation Results

The two-way interleaved ADC proposed in this paper is simulated in a 0.18μm SiGe BiCMOS technology. In this ADC the single core base on a monolithic ADC of 12bits 500MSPS which has fabricated in the same technology and is tested in an 80-pin CQFP package. The simulation is under 1GHz sampling rate and the analog input frequency is 198MHz, The time-interleave spurs without calibration is shown in Fig.4. The gain and timing mismatch will case the spurs at the *f*s/2 ± fin(301MHz,-64dB). The offset of the two-way will case the spur at the *f*s/2(500MHz,-63.4dB). The implemented look table interleaving calibration algorithms reduce the gain and offset spurs, as shown in the FFT plots of Fig. 5. Offset error spur reduced to less than -94dB, gain error spur reduced to less than -106dB after timing calibration.

Finally, the simulation performance of the experimental prototype is summarized in Table 1.

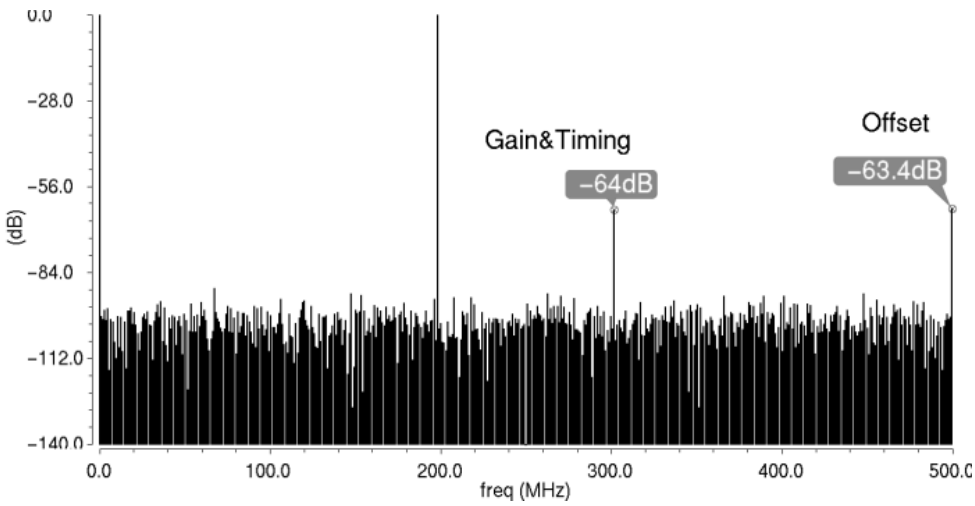

Fig.4. 1024 point FFT at Fs=1GS/s and Fin≈200MHz without calibration.

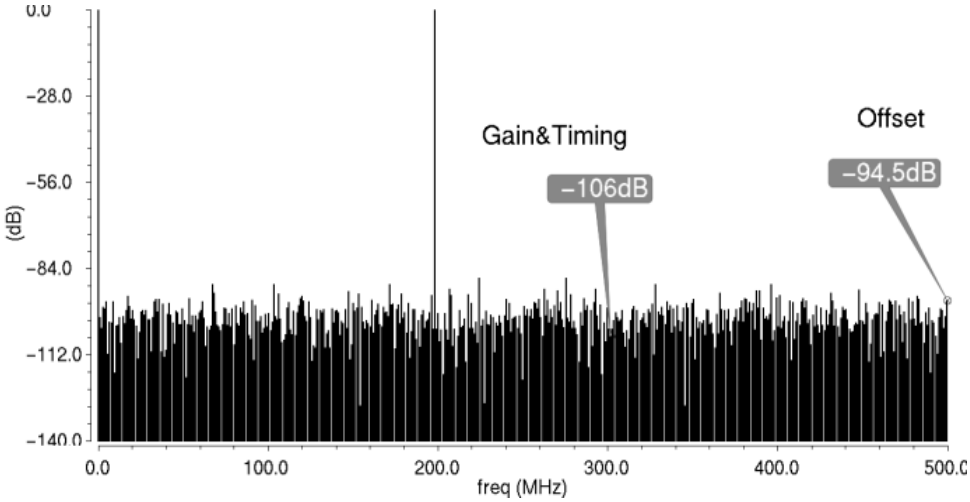

Fig.5. 1024 point FFT at Fs=1GS/s and Fin≈200MHz with calibration.

Conclusions

This paper has presented the design of a 12 bit 1GS/s two-way time-interleaved pipeline ADC which achieves an SFDR of 87dB at 200MHz. To use the OTPNVM the recode correction reduces the gain and offset spurs of the interleaving errors. As a result the largest harmonic in the spectrum is not the channel mismatch error spurs, so that the two channels mismatch is no dominates the time-interleaved ADC performance.

Table 1. PERFORMANCE SUMMARY

Resolution	12bits
Sampling Rate	1GS/s
SFDR	87[dB]
Process Technology	0.18μm SiGe BiCMOS
Power Supplies	1.8[V]
Interleaving Spurs: Gain & Timing Offset	 ＜-106[dB] ＜-94[dB]

References

[1] W.C. Black Jr. and D.A. Hodges, “Time Interleaved Converter Arrays,” IEEE J.Solid-State Circuits, vol. 15, no. 6, pp. 1022-1029, Dec., 1980.

[2] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi, “Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems,” IEEE Trans. Circuits and Systems I, vol. 48, no. 3, pp. 261-271, Mar.,2001.

[3] M.El-Chammas and B.Murmann, “General analysis on the impact of phase-skew in time-interleaved ADCs,” IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 56, no. 5, pp. 902–910, May 2009.

[4] S. Louwsma et al., “A 1.35 GS/s, 10 b, 175mW time-interleaved AD converter in 0.13 m CMOS,” IEEE J. Solid-State Circuits, vol. 43,no. 4, pp. 778–786, Apr. 2008.