A CMOS input buffer with linearization technique for high-speed A/D

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Keywords: Input Buffer, Linearization Technique, High-speed A/D
Abstract. A CMOS input buffer with linearization technique for high-speed A/D is introduced. The buffer features high-linearity and low-power consumption. The simulation shows that the SFDR of the buffer is up to 107dB at an input clock of 250MHz with an input signal of 10MHz. A 14-bit 250MSPS pipelined A/D converter integrated this buffer improves its distortion by 5-10 dB.

Introduction

Input buffer is an essential building block that widely used in A/D converters. And its major challenge is to reduce the charge injection (kick-back) of the ADC sampling capacitances and help achieve the desired linearity.

In order to achieve high input impedance and low output impedance, kinds of linearization techniques[1-2] have been implemented in the literature. These techniques described have their own advantages, but one common failing is that they are not generally suited to CMOS process.

In this paper, we have designed a circuit in standard CMOS process. It proposed a linearization technique for canceling nonlinearities by using track transistor and replica capacitor, which can meet the demands of 14-bit 250MSPS ADC.

The traditional CMOS input buffer

Traditional CMOS input buffer is usually implemented as source-follower as shown in Fig, 1(a). The open loop configuration offers high input impedance and low output impedance, which enable it to isolate the charge injection (kick-back) of the ADC sampling capacitances and the input switch. Meanwhile, low output impedance reduces the distortion caused by the non-linearity in the load impedance and enables a large acquisition bandwidth that helps improve the sampling accuracy and linearity at high sample rates. The only drawback of this circuit is its bad linearity.
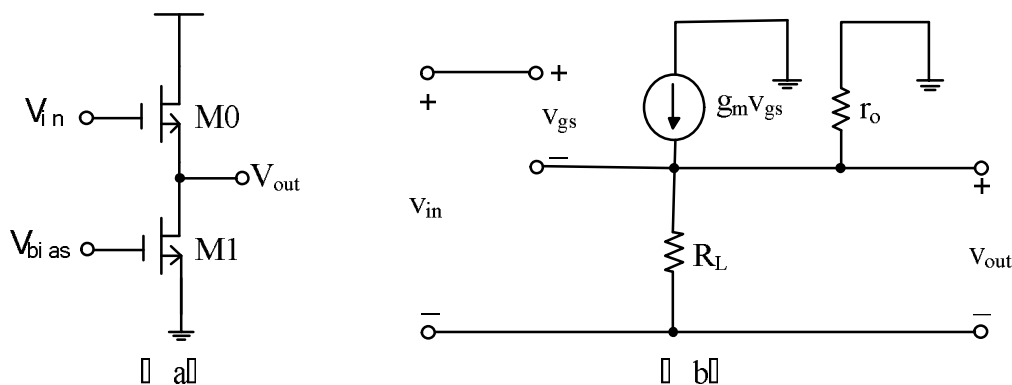

Figure 1. Source-follower(a) and its equivalent circuit(b)

Shown in Fig. 1(b) is its equivalent circuit. The buffer transfer function can be expressed as follows:

$$\frac{V_{out}}{V_{in}} \approx \frac{g_m r_o}{1 + g_m r_o + \dfrac{r_o}{R_L}} \tag{1}$$

Where Vout is the buffer output voltage, Vin is the buffer input voltage, gm and ro are the trans-conductance and output resistance of the NMOS transistor M0, RL is the load impedance.

As the load transistor M1 of the buffer is a current source, that is to say, if R_L is large enough, such as cascode current source, equation (1) can be reduced to

$$\frac{V_{out}}{V_{in}} \approx \frac{g_m r_o}{1 + g_m r_o} \quad . \tag{2}$$

From equation (2), we can see that the major source of non-linearity in source-follower is the variation of transistor parameters gm and ro. Due to channel length modulation[3], gm (or ro) is a function of the drain-source voltage V_{DS}, which depends on the signal current flowing through the sampling capacitance. This variation causes the parameter gm (or ro) to be dependent on the input signal, which leads to distortion.

The traditional approach to improve the distortion in source-follower has been to increase the bias current of M0, so the relative change in current is small enough to achieve the desired linearity. Unfortunately, by this way the transistor parasitic increases simultaneously as the size of the device increases, which eventually limit the achievable linearity. In addition, this approach leads to high power consumption due to the large bias current and supply voltage[4].

The proposed CMOS input buffer

The best way to increase the linearity is to decrease the variation of the drain-source voltage[5]. This is shown conceptually in Fig,2 (a), where an N-type source-follower is added to a basic p-type source-follower to keep the drain-source voltage of the PMOS transistor constant.

Based on this method, we employ a buffer linearization technique that used a capacitor and transistor to track the voltage variation in the source-follower, shown conceptually in Fig,2 (b).
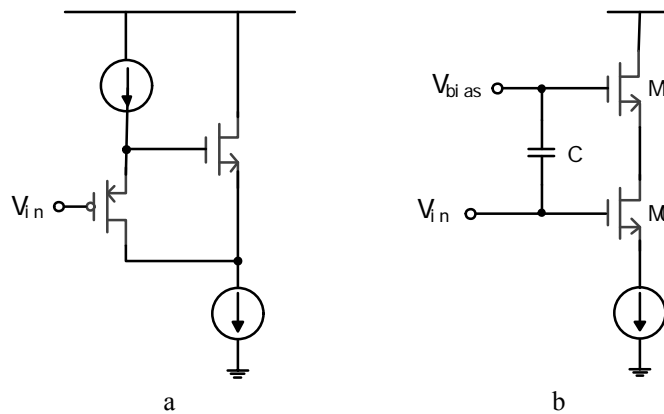

Figure 2. Linearity technique(a)published technique (b) proposed technique

In Fig.2(b), it is obvious that the source and drain of NMOS transistor M0 both track the input signal for ac analysis, resulting in constant V_{DS}. Compared to [5], the idea we propose is simpler because only one circuit branch is needed.

The proposed idea can be implemented with the circuit structure in Fig.3. It is composed of three extra parts besides track circuit (the bias circuit has been omitted for the restriction of the length of the article).
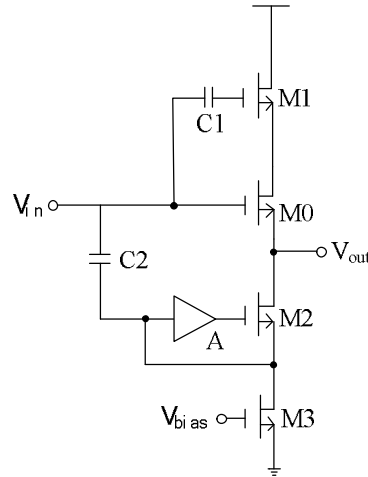
Figure 3. The proposed CMOS input buffer

As mentioned above, gain-boost technique was used to improve the output resistance of the current source. The output resistance can be expressed as

$$R_L \approx A g_{m2} r_{o2} r_{o3} \tag{3}$$

where ro2 and ro3 are the output resistances of the NMOS transistors M2 and M3 respectively, A is the gain of the gain-boost amplifier, and gm2 is trans-conductance of M2. So, the non-linearity of current source load can be ignored.

The third part is a replica circuit. When the input signal is at high frequencies, the current through M0 will still change because additional current is needed to charge sampling capacitor.

In this paper, we add a replica capacitor to inject current to the output node at high frequencies. Because of the cascode transistor M2, the bottom plate of the dummy capacitor is equivalent to be connected to ac ground. The currents through dummy and sampling capacitors are equal to each other because the voltages at both top plats make same change due to the source follower. Consequently, the current through M0 is almost unchanged because the current through sampling capacitor is mainly provided by the replica capacitor.

Therefore, the combination of the three parts yields higher the linearization by compensation of the variation of voltage and current in the source-follower.

Simulation results

The proposed CMOS input buffer has been designed in 0.18μm CMOS process and simulated by Spectre using foundry models. Simulation results show the performance of linearization, which is the main index of input buffer.
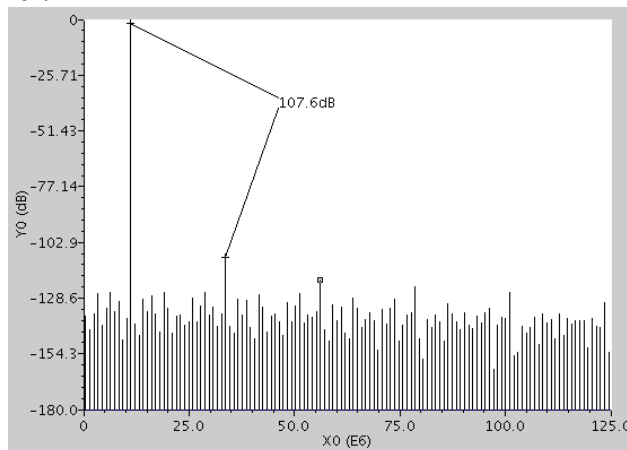

Fig.4 Simulation results

The proposed CMOS input buffer is applied to a 14-bit 250MSPS pipelined A/D with an input signal of 10MHz. Fig.4 shows that the SFDR of the buffer is up to 107dB at TT process corner at temperature 25°C. The simulation shows that the buffer can improve the distortion by 5-10 dB, which meet the demands of 14-bit 250MSPS pipeline ADCs and other high-speed and high resolution ADCs.

Conclusion

This paper has presented a CMOS input buffer circuit in standard CMOS process. The main feature of the design is the proposed linearization technique, which uses track transistor and replica capacitor to compensate the variation of voltage and current in the source-follower. The simulation shows that the SFDR of the buffer is up to 107dB when applied to a 14-bit 250MSPS pipelined A/D with an input signal of 10MHz. This buffer improves its distortion by 5-10 dB.

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