Design and Implementation of Nanosecond Pulse Generator based on Reconfiguration PLL in FPGA

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***Abstract*—Narrow pulses have become an essential requirement in Biology, Chemistry, Communication and other fields. PLL based on dynamic reconfiguration technology in FPGA has been adopted in this work to implement a narrow pulse generator with nanosecond pulse width. The generated pulse frequency and the pulse width are easily adjustable in real time by simply reconfiguring the frequency and the phase shift parameters of the PLL. The realized narrow pulse has a frequency range from 5MHz to 300MHz and pulse width from 1ns to 100ns. The implemented narrow pulse generator has the advantages of small size and flexible controllability when compared with the available standard generators. Thus, the presented work in this paper provides a novel approach to generate narrow pulses with configurable frequency and pulse width.**

Keywords—field programmable gate array (FPGA); phase-locked loop (PLL); dynamic reconfiguration; nanosecond pulse

I. INTRODUCTION

A considerable amount of attention has been devoted to the narrow pulse in recent years, due to the fact that it has widespread applications in a number of different promising fields. For example, pulse power supply can be used to improve the locality of the electrochemical dissolution and to increase the process stability in the micro electrochemical machining (ECM). Moreover, the narrower the pulse width is, the higher the accuracy of the ECM is [1-2]. Narrow pulses are also commonly used to drive LED in spectroscopy measurements for material research [3]. Even electric field aroused by narrow pulses is being used these days to induce apoptosis for the treatment of cancer and other diseases in the Biomedical field [4-5]. Furthermore, narrow pulses with nanosecond pulse width and the following order of magnitude are typically utilized for data communication in the ultra-wideband wireless communications [6-7].

Conventionally nanosecond pulses are generated either by taking advantage of the switching and the current amplifying characteristics of the avalanche transistor [8], or by exploiting the principles of single transmission lines [9]. Since these methods utilize the inherent properties of the avalanche transistor and the transmission lines to generate narrow pulses, therefore, they do not have flexibly adjustable pulse width capability.

For the design and implementation of a narrow nanosecond pulse generator with adjustable frequency and pulse width capability, a novel approach based on the reconfigurable Phase-Locked Loop (PLL) module, available in Field Programmable Gate Array (FPGA), is proposed in this work.

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II. PRINCIPLES OF RECONFIGURABLE PLL

A phase-locked loop (PLL) is a feedback frequency control system. The basic functionality of PLL is to replicate and track the frequency and the phase of the input signal when it is in lock step. The phase and the frequency of the generated output of PLL are directly related to the input signal. Thus, a classical phase-locked loop system is composed of a phase frequency detector (PFD), a voltage controlled oscillator (VCO) and a low pass loop filter (LF). PLL is used in several practical applications with different design criteria but all these various loop designs are derived from the basic loop. The schematic of PLL of Altera Company's FPGA is shown in Fig.1[10], which consists of the above mentioned basic elements along with a pre-divider counter (N), a feedback multiplier counter (M), a charge pump (CP) and a post-divider counter (K).

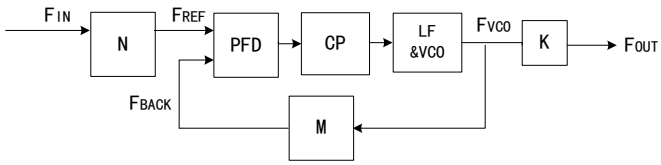

Fig. 1. PLL schematic diagram of Altera FPGA.

PFD compares the reference signal F_{REF} and the feedback signal F_{BACK} to produce an error signal which is proportional to the phase difference between the two signals. The produced error signal is then converted into a correction current signal by the CP module. After passing the loop filter, a corresponding control signal is generated to regulate the oscillation frequency of the voltage-controlled oscillator (VCO) within its tuning range. The F_{VCO} signal is fed through M module back to the input of the PFD block as F_{BACK} shown in Fig.1, forming a negative feedback loop. As a result of this loop, if the F_{REF} signal and the F_{BACK} signal are coherent then the PLL is said to be phase-locked. The insertion of the M, N, K counters ensures the accomplishment of a broad frequency range F_{OUT} signal.

Consequently, the frequency of the F_{REF} signal is described by

$$f_{REF} = f_{IN} / N \quad (1)$$

The output frequency of VCO is described by the equation

$$f_{VCO} = f_{IN} * M / N \quad (2)$$

And the final frequency of PLL is given by

$$f_{OUT} = f_{IN} * M / (N*K) \quad (3)$$

Due to the fact that a suitable mechanism of providing registers is required to store the component parameter values, a dynamic reconfiguration feature of the PLL has been marketed which allows the real time dynamical adjustment of the output phase, the frequency and the bandwidth. An ALTPLL IP core of PLL [11] in Altera FPGA is shown in Fig.2 illustrating the internal registers and pins.

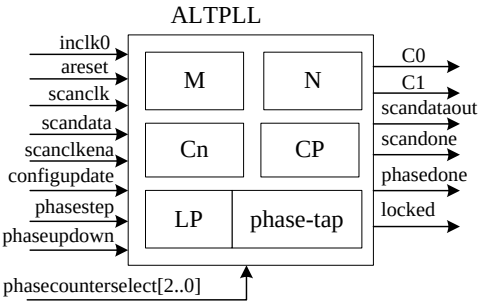

Fig. 2. Registers and pins for reconfigurable ALTPLL IP core.

In case for the internal registers, the output frequency and its duty cycle can be modified by changing the pre-divider parameter (N), the feedback multiplier parameter (M) and the post-divider parameter (Cn). The output phase can be amended simply by varying the output phase adjustment parameters (phase-tap). The adjustment in the charge pump parameter (CP) and the resistance, the capacitance parameters of the loop filter (LP) can cause affective variation in the output bandwidth.

To the external surfaces, the frequency and the phase can be reconfigured by utilizing the controlling pins *areset*, *scanclk*, *scandata*, *scanclkena* and *configupdate*. In addition, the *phasestep*, *phasecounterselect[2:0]* and *phaseupdown* pins can be used to configure the phase only. The C0 and C1 pins shown in figure 2 are the two channel outputs of the PLL. The *scandone* and the *phasedone* both are output status flag pins to indicate the completion status of the scan and the phase configuration respectively. The *scandataout* is the data output port for the serial scan chain and can also be used to determine when the reconfiguration is completed because the last output is cleared once the reconfiguration is finished. The locked pin is also a status flag pin to indicate the PLL locked state. The locked pin is low when PLL is out-of-lock and gets high once the PLL is locked.

Altera Company also provides an ALTPLL_RECONFIG IP core with parallel-serial conversion and decode capabilities in order to facilitate the dynamic real-time reconfiguration of PLLs. This IP core offers the reconfiguration logic for PLLs on one hand and the surface logic for users on the other hand.

III. THE GENERATION OF NANOSECOND PULSES

A novel and compact approach to generate nanosecond pulses has been employed in the presented design. The first step is to produce two clock signals with the same frequency but different phases. The second step consists of executing the logic operations as follows: C = A *or* B and then D = C *xor* A. As demonstrated in Fig.3, D is the desired narrow pulse signal. Meanwhile, the adjustment in the frequency of the first two signals (A and B) and the alteration in the phase of the second signal (B) will result in the change of the frequency and the width of the output narrow pulse respectively.

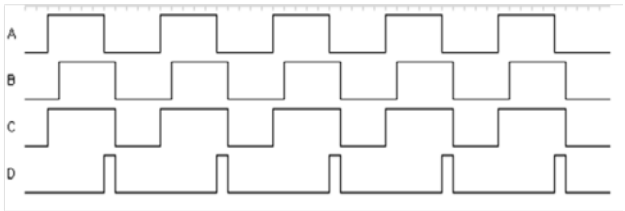

Fig. 3. Timing diagram of the logic operations.

Figure 4 shows the block diagram of the structure of the nanosecond pulse generator system. Once the reconfigurable PLL module produces two original clock signals A and B, the phase control module modifies the phase of the PLL output signal B with respect to signal A. At the same time, the frequency control module modifies the frequency of the two signals together and this is where an ALTPLL_RECONFIG module is introduced to aid the real-time dynamic reconfiguration of the PLL module.

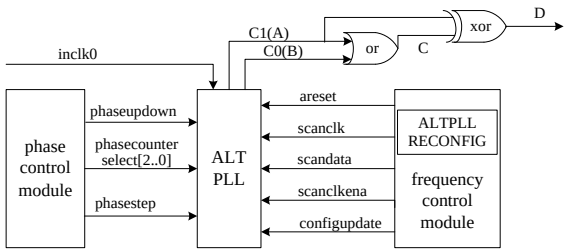

Fig. 4. Structural black diagram of the System.

A. Phase Reconfiguration

The phase control module is elaborately organized to time the three main control signals (*phasestep*, *phaseupdown*, *phasecounterselect[2:0]*) of the PLL module for the phase shift of C0 output signal with respect to C1 signal. Figure 5 explains the timing of the dynamic phase shift process.

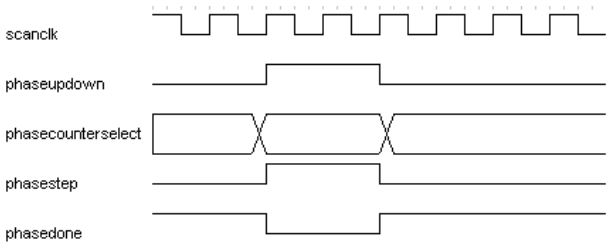

Fig. 5. Timing diagram of the phase reconfiguration..

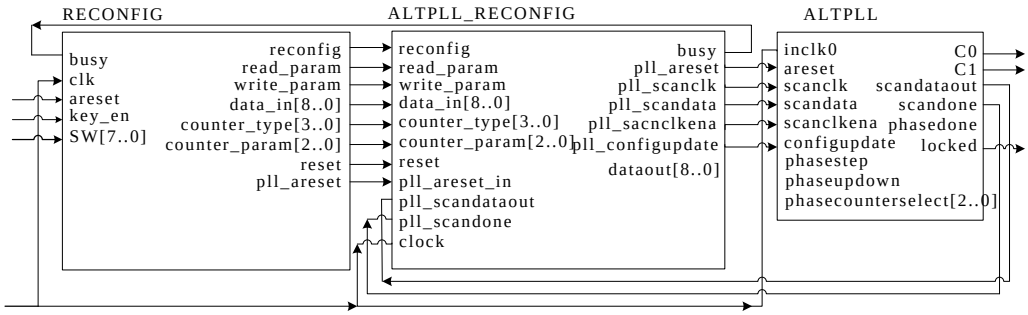

Fig. 6. Block diagram of the frequency reconfiguration structure.

Where, *phaseupdown* is a dynamic phase shift direction signal to specify the adjustment direction either up or down. Selecting up will direct the PLL to shift back by a factor of $1/8^{th}$ of the time period of the VCO at each step. Whereas, selecting down direction will imply that the PLL will shift forward by the same factor of 1/8th which denotes that the phase shift step resolution is directly proportional to the frequency of F_{VCO}. The *phasecounterselect[2:0]* is a three-bit counter select bus to select the PLL clock counter, such as "011" aimed to select C1 counter. The *phasestep* is a dynamic phase shift active high enable signal to activate the phase shifting. Since a single pulse signal will only allow a single phase shift adjustment, therefore, if one wants to have a large phase shift, he just needs to make several adjustments and they all will accumulate at the end. The *phasedone* signal indicates that the dynamic phase reconfiguration is completed when asserted. The signal *scanclk* is a synchronous clock signal for the serial scan chain.

It is worthwhile noticing here that once the PLL resets, the FPGA programming file will decide to set the phase relationship to its initial state which can lead to invalid phase adjustment.

B. Frequency Reconfiguration

A module named RECONFIG is designed to reconfigure the frequency of the ALTPLL module with the use of an ALTPLL_RECONFIG module that acts as a bridge between the two modules. The connections among three modules are shown in Fig.6.

To alter the output signal frequency described in Eq. (3), the reconfiguration of the M, N and K parameters is required keeping the input clock signal fixed. The timing diagram for the parameter reconfiguration is illustrated in Fig.7. Meanwhile, the configuration process can be described by the following steps.

(1) With the 4-bit *counter_type* port, specify a counter type (C0-C4, M or N).

(2) Use the 3-bit *counter_param* port to identify the parameter that should be updated for the counter type.

(3) The 9-bit *data_in* port is used to provide value for the parameter selected by the *counter_param*.

(4) Assert the *write_param* signal for one *scanclk* cycle to allow the above mentioned three inputs to be written to the scan chain.

(5)The busy signal is asserted as soon as the *write_param* signal is asserted until the parameter has been written.

(6)Once the busy signal is de-asserted, other parameters can be written. When all the parameters are shifted into the scan chain, assert the *reconfig* signal for one *scanclk* cycle to update the PLL.

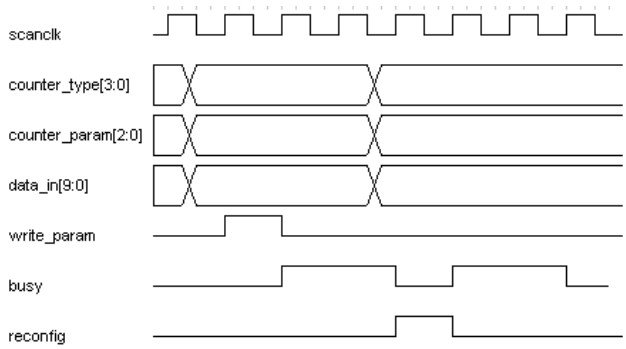

Fig. 7. Timing diagram of the frequency reconfiguration.

IV. EXPERIMENTAL RESULTS AND OUTLOOK

The proposed system framework for nanosecond pulse generation is implemented on DE_115 development board that includes the Cyclone IV FPGA chip with external input clock frequency of 50MHz. The accomplished narrow pulse with dynamically adjustable frequency and phase capability has the frequency range from 5MHz to 300MHz and variable pulse width from 1ns to 100ns. The versatility of the proposed system allows users to adjust the design according to their own requirements for frequency range, accuracy of phase and so on subjected to various applications.

It shows the three resultant signal waveforms acquired by logic analyzer Agilent 16823A. In Fig.8 the frequency of the signal D is 10MHz and the pulse width is 1ns. Fig.9 shows the resultant signal D with 10MHz frequency and 4ns pulse width. The third and last signal D is illustrated in Fig.10, having a 5MHz frequency and a pulse width of 4ns.

The produced nanosecond pulses belong to low-power pulse signals. As the amplitude magnitude and the driving capability of the pulse signal theoretically depend upon the FPGA's I/O (input/output) standards. Therefore, the electro-optical and the photoelectric conversion methods which are

under consideration currently by the researchers to achieve decent power amplification of narrow pulse signals will be investigated in the future work.

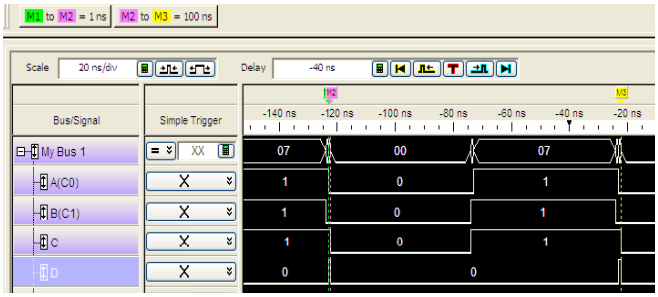

Fig. 8. Frequency10MHz and pulse width 1ns.

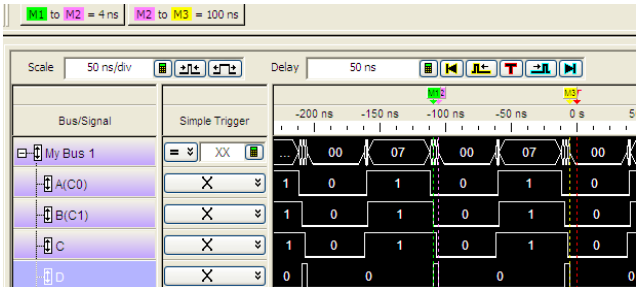

Fig. 9. Frequency 10MHz and pulse width 4ns.

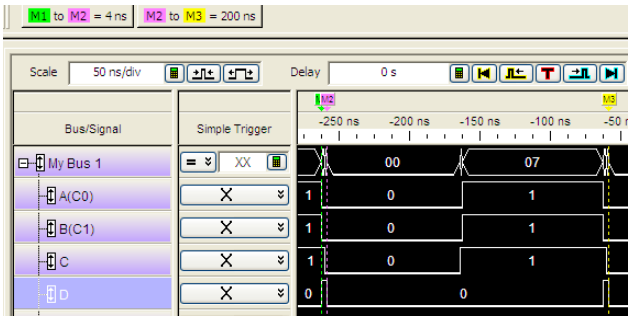

Fig. 10. Frequency 5MHz and pulse width 4ns.

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