A Novel 8T SRAM Cell with Improved Read and Write Margins

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Abstract. A highly stable 8T SRAM cell is presented to improve the Static Noise Margin (SNM). The proposed 8T SRAM cell uses a single-bit line structure to perform read and write operation. The design enhances the write ability by breaking-up the feedback loop of the inverter pair. It also improves the read stability by eliminating the effects from the bit-line. The simulations show that the proposed 8T cell offers 2.07x read static noise margin, 1.41x and 2.60x in write '0' margin compared to the conventional 6T cell and 7T cell, respectively. Besides, the proposed structure has a significant improvement in writing '1' operation and HSNM.

Introduction

According to ITRS road map, memory chips SRAM arrays will occupy most of the chip area in upcoming years. In order to achieve higher speed, performance and lower power consumption, the CMOS process technology is continuously scaling. Since the supply power has a significant impact on power consumption, voltage scaling is one of the most effective techniques for power reduction in digital VLSI design. However, it has some limitations like loss of static noise margin (SNM). And current fluctuations due to process variations and limitations on the number of cells connected to a single bit-line [1]. In the conventional 6T SRAM cell, the structure has a severe problem of read disturbing. One basic and effective method to eliminate this problem is the decoupling of true storing node from the bit lines during the read operation [2].

To improve the performance and data stability, several structures [3,4,5] have been proposed at the cell level. For instance, a new 7T cell is proposed in [3], which improves the stability of the SRAM cell and reduces the average power dissipation during the read write operation and reduces the leakage power in standby mode. The usage of new devices such as FinFETs [6,7] has been suggested to improve the performance. In [6], the 8 SRAM cell structure was studied based on the 5nm FinFET technology. This technique significantly increased the WM and has no adverse effect on the read SNM. Besides, the researchers have developed new methods [8,9,10] to decrease power consumption.

A novel 8T SRAM cell is presented in this paper, using a single-bit line for read and write operations. The main contributions of the paper are listed as follows. First, the proposed cell improves both read and write noise margin as comparison with the conventional 6T SRAM cell. Second, the design only utilizes one bit line. Finally, compared with 6T SRAM cell, the proposed 8T SRAM cell has lower power consumption.

The rest of the paper is constructed as follows. The principal of the proposed 8T SRAM is reviewed in section two. In section three, the simulations results are presented and discussed. And section four concludes the paper.

8T SRAM Cell Design

The schematic of the proposed 8T SRAM cell is presented in Fig.1 which uses single bit-line for read and write operations but has an extra world-line (RWL) for read. For a conventional 6T cell the worst-case Static Noise Margin (SNM) occurs in the read condition. This structural change is to improve the stability of the cell and eliminate the read disturb existing in the conventional 6T SRAM cell. In this SRAM cell design, transistor P3 is used to enhance the write margin and low power

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consumption of the circuit by breaking-up the feedback loop of the inverter pair. In next two subsections, we will introduce the operating principles of the proposed 8T cell in detail.

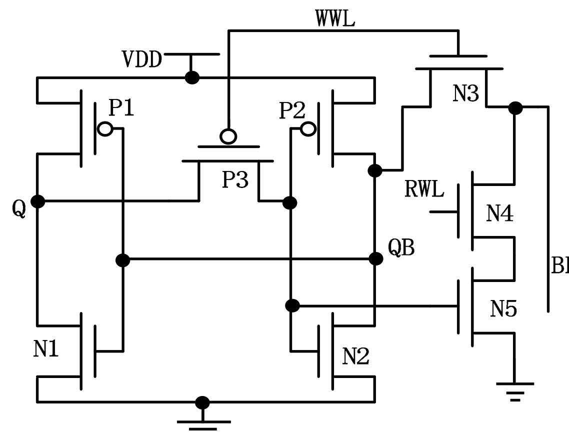


Fig. 1 The proposed 8T SRAM cell

Write Operation. A single-ended write design has comparative degradation in write performance in comparison to the conventional write structure using complementary bit-line pair. Nevertheless a dynamic mechanism of cutting feedback loop can effectively improve the write ability in the proposed 8T cell. In the write operation, WWL is set to VDD to prepare a path from internal node 'QB 'to BL and break the feedback loop. The RWL is set to VDD in the entire write operation.

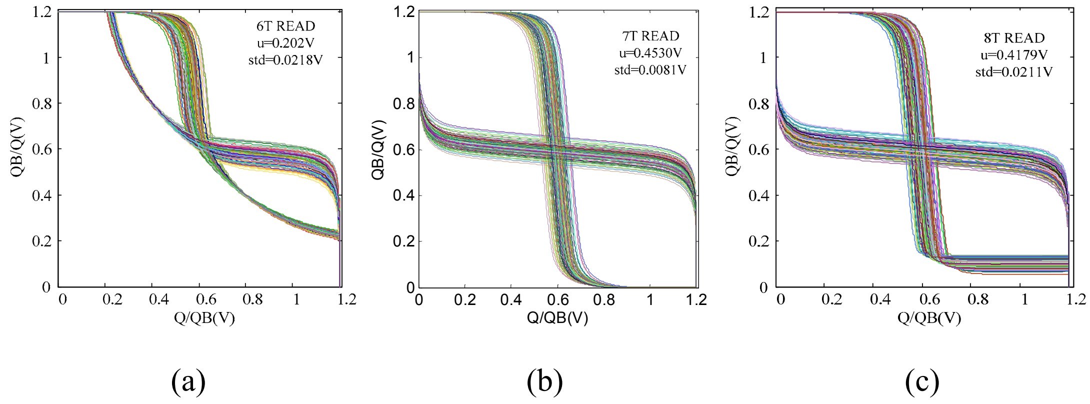
During write '0' operation, WWL is attached to high, while BL and RWL are at ground which can switch transistor N4 and N5 off. If '1' is stored at node 'QB', the gate of the transistor N2 will be pull down the ground and the node 'QB' retains at very low voltages instead of 0V. Thus the transistor P1 turns on and it pulls up the voltage of storage of node 'Q'. On the other hand, during writing '1' operation, both RWL and BL are at ground and the voltage of 'QB' is pull up using transistor P2, which can force QB to change the state from '0' to '1'.

Read Operation. In our proposed 8T SRAM cell, the stored nodes are decoupled from the bit-line which eliminates the read disturb and presents better RSNM compared to the conventional 6T SRAM cell. For the read operation, the BL is pre-charged VDD initially. We can judge the stored data by depending on the state of BL. The proposed 8T SRAM cell improves the RSNM by at least 2.06x and as compared with conventional 6T SRAM cell. During the read operation, the bit-line is pre-charged to VDD, RWL is set to high. The WWL is set to low in the entire read operation, which turns off and turns on N3 and P3. As 'Q' node stores '1' logic (Q= '1', Q= '0'), the transistors N2, N5 and P1 are on and N1 as well as P2 is off. The BL discharges through N4 and N5 to the ground. Similarly, when 'Q' stores '0' logic (Q= '0', QB= '1'), the transistors P2 and N1 are on and P1, N2, N5 are off. Thus, there is no discharging path from BL to ground.

Simulation Results and Comparison

In this section, simulation results have been obtained among conventional 6T, 7T and the proposed 8T SRAM cell. The RSNM and WM will be discussed in the section. All simulation results are done at SMIC 65nm technology.

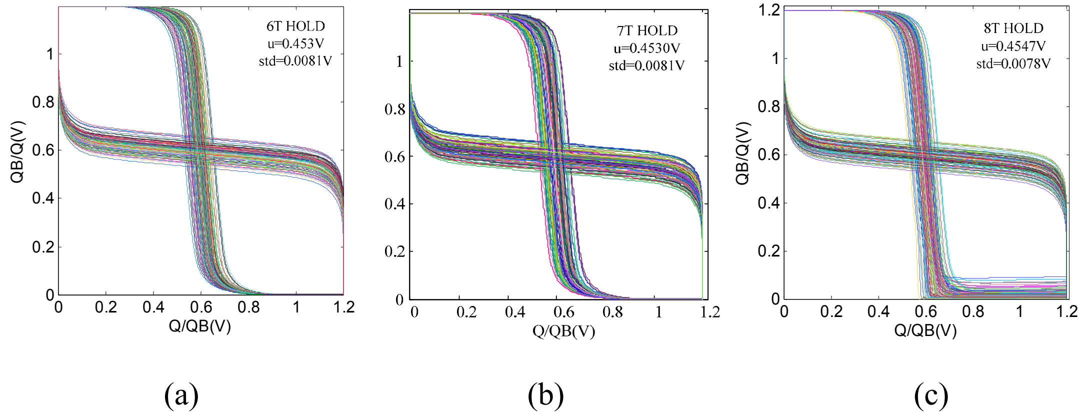
Read Static Noise Margin (RSNM). As shown in Fig. 2, the analysis of the RSNM is based on 2000 samples Monte Carlo simulations during the read operation. The butterfly curves of 6T, 7T and 8T SRAM cells are shown in (a), (b) and (c) of Fig.2 respectively, which indicate the read ability. The statistic shows that the proposed cell presents 2.06x improvement in RSNM as compared to 6T SRAM cell. Obviously, the proposed 8T cell is superior to the 6T cell in read operation.



(a) (b) (c)

Fig.2 Read butterfly curves of SRAM cells

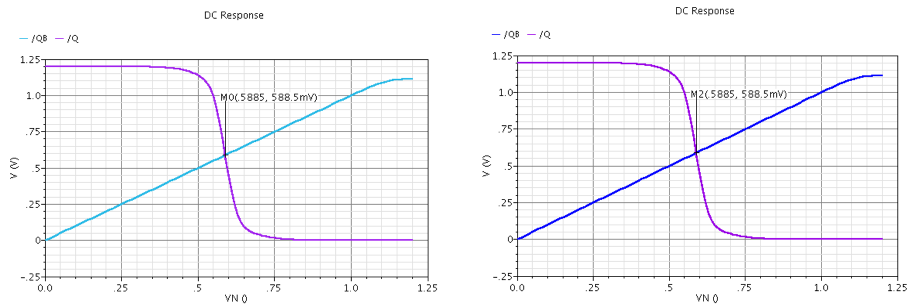
Hold Static Noise Margin (HSNM). Fig.3 shows the noise margin comparisons of SRAM cells during data retention. All statistical butterfly curves of SRAM cells have been carried out 3000 Monte Carlo simulations samples at low supply power. As shown in (a) and (b), the simulation results shows the 7T is similar to 6T cell in hold mod. But our proposed design (c) offers better hold stability and the lowest deviation as compared to 6T cell and 7T cell.



(a) (b) (c)

Fig.3 Hold butterfly curves of SRAM cells

Write Margin (WM). This new structure improves WM significantly, especially in writing '1' operation. As depicted in Fig. 4, the write '0' of our proposed design is enhanced (1.41x and 2.6x as compared to 6T and 7T).



(a) 8T Write '0' margin (b) 8T Write '1' margin

Fig.4 WM of 6T, 7T and 8T

Power Consumption. TABLE I compares the read, write and hold power consumption of 6T, 7T and proposed 8T SRAM cells. The experimental results show that the average power consumption of the proposed design is lowest as compared to 6T and 7T.

Table I Power Consumption of Different Cells

SRAM cell	Read'0'(W)	Read'1'(uW)	Write'0' (pW)	Write'1'(W)	Hold (pW)
6T SRAM	52.69u	52.69	103.8	103.8p	139.8
7T SRAM	136p	52.68	143.6	52.69u	179.6
8T SRAM	1.109n	52.68	104.8	598.1p	143.2

Summary

A novel single ended 8T SRAM cell with high stability is proposed in this paper. The proposed cell has been found to perform better in read and write operations. While performing the write and read operation, the design enhances the WM and RSNM respectively. It breaks up the feedback loop of the inverter pair and obtains an excellent read robustness. Compared to the conventional 6T SRAM cell, the proposed cell exhibits 2.07x read static noise margin and 1.41x write margin. Besides, lower read and write power dissipation is obtained in this new structure.

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