Design of IVS Based on the Davinci DM6446

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***Abstract*-The technology of Davinci contains Davinci processor, related software, development environment, algorithm library and some other technical support. This paper designs the software and hardware to complete the intelligent Video Surveillance such as motion detection, self-tracking, analysis and determine by using the dual-core processing chip TM320DM6446. It modifies the target detection algorithm which has been achieve on PC, and it controls the PTZ by target offset. This scheme adopts the monolithic system, and it has some advantages such as simple design, good extension, reconfigurable algorithm.**

Keywords-Davinci processor, Intelligent Video Surveillance, Motion detection, self-tracking, analysis and determine

I. INTRODUCTION

As the increased demand for security and rapid expansion of monitoring information, using artifical way to monitor video surveillance already connot satisfy regulatory actual demand. Intelligent video surveillance includes lots of motion detection, self-tracking, data compression and other algorithms, and it should has high requirement on real-time, also need computing-powerful processor and a lot of external storage support. So it is suitable for DSP. And for the controlling of collection of external data and terminal display, it is more suitable to use ARM processor. So we choose the processor TMS320DM6446.

TM320DM6446 which is dual-processor can reach the speed of 4800MIPS, and it can well solve the above contradictions. DM6446 integrate two processors of C64+DSP and ARM926EJ-S. DSP complete motion detection, algorithm of video data compression alone, ARM processor complete controlling of the whole system, both work together collaboratively [1] .

II. GENERAL STRUCTURE OF THE SYSTEM

This system consists mainly of image acquisition module, image processing module, image storage module, as show in Figure.1.

The system is controlled by the ARM side of DM6446, the algorithms are completed by DSP side. The collested video signal complete A/D conversion by TVP5158 and then sent directly to VPEF. The DSP side analyses of and processes the digital video signal by using intelligent detection algorithm, and then compresses the processed video signal [2].

The DM6446 is connected to a 256M 32-bit DDR memory controller. It uses voice alarm mode, by using the serial audio interface connection audio encoders to achieve. In orde to stroe the compressed video signal, 40G hard disk is connected to DM6446 through ATA controller. Ethenet port is to send the compressed video signal, USB is used to debug the system, SD card can upgreding the system. The develops write applications to control the PTZ. CVBS output is to connect the system and monitor.

III. THE MAJOR HARDWARE DESIGN OF SYSTEM

The hardware of this system mainly contains power module, image acqusition module, network modul. This section mainly talk about the image acqusition module. It mainly contains the seamless between TVP5158 and DM6446. The components of the system requires several different power supply voltage, 1.2, 1.8, 3.3, 5 V. So it needs a voltage conversion module include TPS54231, AP1117E18L-13, AP1117E33L-13. Network module mainly composed of Ethernet transceiver KSZ8041NL and network transformer HE-MX2061.

The TVP5158 device is 4-channel, high-quality NTSC/PAL video decoder that digitizes and decodes all popular base-band analog video formats into digital video output. Each channel of this decoder includes 10-bit 27-MSPS A/D converter. Preceding each ADC in the device, the corresponding analog channel contains an analog circuit that clamps the input to a reference voltage and applies the gain. Video output ports support 8-bit ITU-R BT.656 and 16-bit 4:2:2 YCbCr with embedded synchronization. TVP5158 supports multiplexed pixel-interleaved and line-interleaved mode video outputs with metadata insertion [3]. The connection diagram between TVP5158 and DM6446 is Seamless， as show in Figure.2.

IV. THE DEVELOPMENT ENVIRONMENT AND RELATED PACKAGES

First building montavista environment, then installing TI DVSDK tool chain, and then installing Codec Engine, last completing the dual-core communication environment [4].

DSP/BIOS is a real-time operating system created and offered by Texas Instruments for use in a wide range of DSPs and microcontrollers. C6x Code Generation Tools is a real-time DSP system. DSP/BIOS LINK is foundation

software for the inter-processor communication across the GPP-DSP boundary. dsplinkk.ko is a pre-configured, pre-built DSP Link driver. Cmemk.ko is a Contiguous Memory allocator that allows allocation of physically contiguous buffers of arbitrary sizes (even several MB) on the GPP. XDC Tools like the gmake tools. XDAIS is algorithm interface standard.

V. ACHIEVING ALGORITHM USING CODEC ENGINE

In developer's opinion, the Codec Engine is a set of APIs using to run xDAIS algorithms. A VISA interface is provided as well for interacting with xDM-compliant xDAIS algorithms. The application calls the core Engine APIs and the VISA APIs. The VISA APIs use stubs to access the core engine SPIs(System Programming Interfaces) and the skeletons. The skeletons access the core engine SPIs and the VISA SPIs. The VISA SPIs access the underlying algorithms, as show in Figure.3.

The Codec Engine has several customer use cases, from GPP-side application developers to DSP-side codec authors. There aer mainly three user rules when using Codec Engine. They are algorithm creater, server integrator, application author.

The Algorithm Creator is responsible for creating an xDAIS algorithm, and providing the necessary packaging to enable these algorithms to be consumed and configured by Codec Engine. For example, in the script of VIDDEC_COPY.xdc we can see:

metaonly module VIDDEC_COPY inherits ti.sdo.ce.video.IVIDDEC

VIDDEC_COPY declares that it is a VISA video decoder algorithm. This allows the Codec Engine to automatically supply default stubs and skeletons for transparent execution of DSP codecs by the GPP [5].

The Codec Server integrates the various components necessary to house the codecs and generates an executable file. For example in the script of video_copy.cfg we can see:

var Server = xdc.useModule('ti.sdo.ce.Server');

Server.threadAttrs.priority = Server.MINPRI;

var LogServer = xdc.useModule('ti.sdo.ce.bioslog.LogServer');

The above statements cause the Server module in the ti.sdo.ce package to be available to the configuration script. It then sets the threadAttrs.priority attribute of the Server module to Server.MINPRI. This indicates that the task threads created by the Codec Server should run at the minimum priority level [6].

The Application Author is responsible for building the application code, and linking into the executable image. Since Codec Engine doesn't perform any I/O, the application is responsible for handling I/O. This includes such task as file access (for example, open/read/write/seek/close) and driver interaction (for example, open/close/ioctl and buffer management) [7]. In this design we should write application, as show in Figure.4.

VI. SUMMARIES

Intelligent Video Surveillance based on DM6446 makes full use of ARM and DSP, and the peripheral circuits is simple, the software structure is clear, the algorithm is reconfigurable. It can complete motion detection, self-tracking, voice alarm, and video storage. It can be wildly used in traffic monitoring, security system and some other ares that need monitoring.

ACKNOWLEDGMENT

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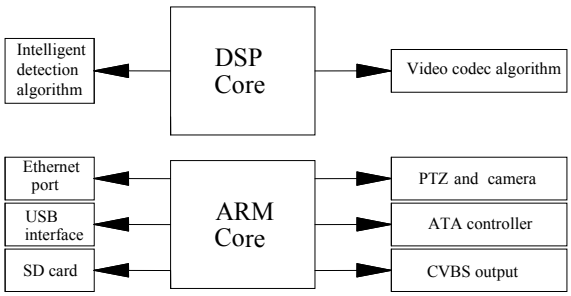

Figure 1. System block diagram

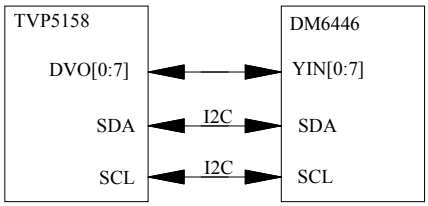

Figure 2. TVP5158 seamless connection diagram

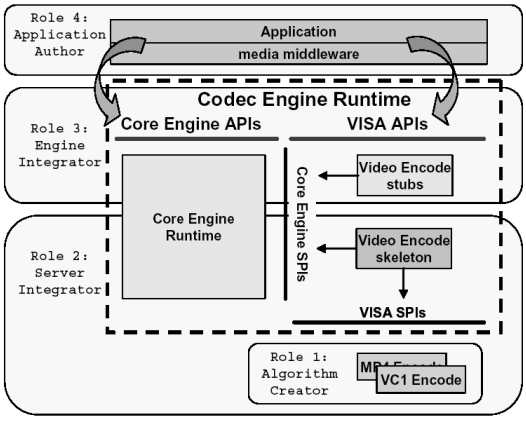

Figure 3. VISA APIs call diagram

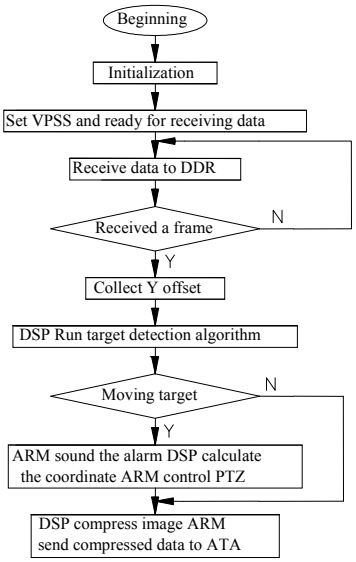

Figure 4. Application flow diagram