Design for Data Collection Circuit of Accelerometer in SINS Based on FPGA

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Abstract. The data collecting method has been studied. The use of large-scale field programmable gate array (FPGA), high-precision programmable A/D converter initialization and data reading have been achieved, in order to obtain a rapid acquisition SINS accelerometer data. The temperature changes will affect the data acquisition precision of A/D conversion circuit. Based on temperature experiment, temperature compensation model is built for A/D converter circuit. The results show that the accuracy of the data acquisition is $5 \times 10\text{-}5g$.

Introduction

As a main inertial instrument of Inertial Navigation System, accelerometers directly affect the accuracy measurement of inertial navigation system [1]. High-precision systems generally use charge-balance type current/frequency converter (I/F) method; while in the low-precision systems, researchers often consider using the A/D conversion method with low cost and small size.

SINS connects the sensitive devices on carriers, which significantly reduces the complexity of the system, and increases the complexity of system computation and real-time property. It requires the use of sensitive device with high impact resistance, wide dynamic range, and fast reaction speed. SINS system is a real-time dynamic navigation system, which has a strong real-time capability in gyro and accelerometer data acquisition, system error correction and system information processing. It is demanding in terms of information processing speed of the system. Therefore, in the acquisition of the gyro and acceleration data, one should complete as much as possible through peripheral logic circuit, so that the DSP have more time for the system solver and error compensation calculation. The paper carried out a detailed analysis on the SINS system acceleration meter data collection process by using FPGA initialization precision A/D converter and data acquisition; its data acquisition accuracy has reached $5 \times 10\text{-}5g$, which has laid the foundation for the rapid processing of system information. Besides, it could also conduct accelerometer error analysis, and create the temperature compensation model and real-time compensation.

Principle of accelerometer signal acquisition

SINS is composed of three accelerometers and three gyroscopes [2]; in the INS solver, it requires that each gyro and accelerometer data acquisition must be done at the same time; therefore, the accelerometer data collection requires simultaneous sampling of three accelerometers. The principle of accelerometer data collection is shown in Fig. 1. The system uses a quartz immunity accelerometer, and outputs an analog current signal. According to the system requirements, the detection accuracy of the accelerometer has reached about $5 \times 10\text{-}5g$. According to the formulas of A/D converter that convert accuracy, researchers have:

$$\frac{U_{max}}{U_{min}} = 2^N - 1 \qquad (1)$$

Where: U_{max} and U_{min} are maximum and minimum of input acceleration signal; N is the digits conversion to 2 decimal. According to the system accelerometer range (-10g ~ + 10g) and precision (5 ×10-5g) requirements, it can obtain A/D converter median:

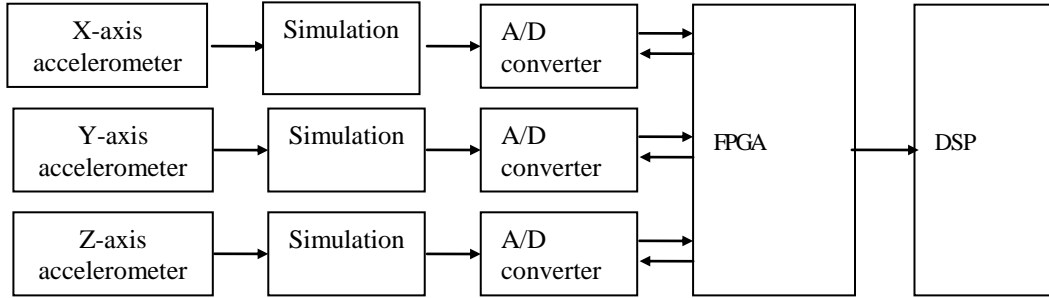$$N \geq \log_2(1 + 2 \times 10^5) = 18 \qquad (2)$$

Fig. 1 Principle Diagram of Data Collection of Accelerometer

Thus, it requires A/D conversion precision should be greater than 18 digits; while, according to the system requirements on accelerometer acquisition rate, researchers set the data acquisition period be 500μs. For such a high conversion accuracy, it is unable to meet the requirements by using the conventional A/D; one must use high-precision A/D converter; if the A/D converter uses a parallel A/D, it will make too many connections between A/D and FPGA chip, but also requires enough pin FPGA chips, which will bring a lot of troubles to hardware wiring, hence researchers use the serial 24 high-precision A/D converter AD7734. The chip is Δ-Σ type A/D converter with high-precision, wide dynamic characteristics [1], and high conversion accuracy. Within the chip, there is a microprocessor: during signal analog to digital conversion, it also completes the signal filtering clean-up, and greatly improves the conversion accuracy of the signal. Therefore, the conversion accuracy is related to the A/D conversion rate. When the conversion rate is 2 kHz, it can reach 19 digits of the resolution, fully meeting the system request on A/D converter.

Design of Accelerometer A/D Signal Acquisition Circuit

A/D Initialization Design. AD7734 is a programmable A/D converter; before use, one must first read its instruction register, the output data register, command register, compensation correction register, and full-scale registers, which are commonly referred to as initialization. A/D initialization process and the data output are completed by the chip DRDY, SCLK, CS, DIN and DOUT pins, mainly involves setting for conversion accuracy, slew rate, input range, gain and data output format; the setup process is more complex, and in the data reading process, it requires an data shift clock provided by external; if the DSP is adopted to perform A/D initialization process and provides data output clock, DSP will take too much computing time. Therefore, the initialization of the A/D converter is done directly by the FPGA.

During the AD7734 initialization, one need to set four registers: each register is three bytes and 24 digits, a total of 12 bytes. When setting, researchers can set a byte one time or 4 bytes one time. Therefore, during initialization, researchers need to divide the 12-byte into three groups according to the register address and each has 4 bytes. According to A/D initialization format requirements, when setting the register, first, one gives an instruction byte to set format, the register address and the number of bytes of data for initialization, and then re-export register settings data, hence each group has a total of 5 bytes 40-bit data of initialization data. Register settings are completed under the control of the chip DRDY signal; when DRDY is low, it is indicating that the chip is ready to receive data, and the external will provide synchronizing clock signal SCLK and input initialized serial data to the chip

SDIO interface; as long as DRDY gives a low electric level, it completed a set of data initializing. So after three set design cycles, the initialization of A/D converter can be completed.

By using FPGA to complete the A/D register initialization process, it is compiled from hardware description language (VHDL language) [3, 4]. Firstly, the author used a counter to design a digital single-shot, and used the falling edge signal of DRDY signal as a trigger for generating one-shot control signal. The one-shot controlling data will control the counter to generate 40-digit initialization clock signal SCLK; at the same time, re-use monostable control signal to control a two-digit counter, so as to generate initialization data switching control signal and control the data output of three groups in order. The initialized data will be set directly in the FPGA, and then latched into the shift register; the shift clock signal SCLK controlled the shift register serial output data signal. Initialized data is exported only in the first three cycles of data. After the first three cycles, there will be no output data, and it will maintain a high electric level, while the clock SCLK has remained unchanged. After the first three cycles, the clock signal will be used as A/D converter data to output clock, until the direct control of the output data. While the initialization takes up a lot of FPGA resources, because FPGA is the digital logic circuit, each part of the timing circuit is completely independent, so it does not affect the acquisition circuit timing relationships of other information.

A/D Conversion Data Reading. Output of AD7734 conversion data is also controlled by control signal DRDY: when DRDY is low, A/D conversion data is ready, then SCLK will output clock signal, A/D conversion data is exported from the DOUT output port of the chip; after the end of data output, DRDY goes automatically to high electric level. Data reading into circuit mainly completes string conversion of data, and signals an interrupt signal to the DSP after string conversion. Converting data will be read once for all through the bus. Because of synchronous mode of A/D data output, the reading process is relatively simple: directly use the synchronous clock SCLK as a serial shift clock, convert the data to parallel data, and use the rising edge of DRDY signal as parallel data lock signal and trigger signal by DSP interrupt, so as to trigger DSP to read switching signal. Timing of reading and writing signal could be seen in Fig. 2and Fig. 3.
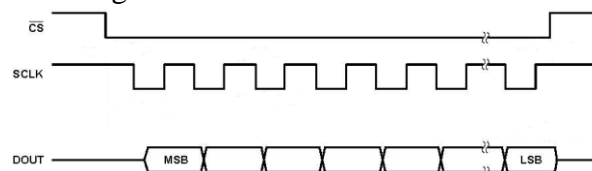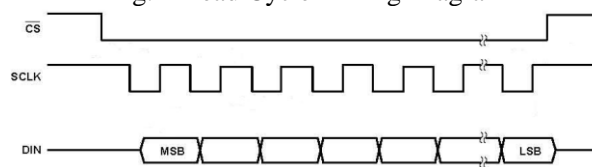
Fig. 2 Read Cycle Timing Diagram

Fig. 3 Write Cycle Timing Diagram

Temperature Compensation Model Analysis of Accelerometer A/D Converter

The output precision of high resolution A/D conversion chip is greatly influenced by temperature drift, linearity and other factors; it must be compensated in system applications. The following will study the effects and compensation of A/D converter circuit temperature changes on static accelerometer output.

Design of Temperature Measuring Circuit. Each A/D chip is installed with platinum resistance, as shown in Fig. 4, it uses the constant voltage temperature measurement circuit, which is composed of the platinum resistance temperature detector, temperature electrical part bridge, DC amplification circuit and so on. Wherein the resistance R1, R2, R3 and Rt platinum resistance compose Temperature Bridge; a point of the bridge provides through 14digits ADC (AD7863) and provides voltage of 2.5V, when the temperature resistance Rt varies with temperature, the output voltages b and c in the bridge

will change. After the bridge output voltage is enlarged by U1B amplification, it will be sent directly to AD780 for analog digital conversion; each point temperature changes are recorded after the navigation computer data acquisition, and processing. Integrated operational amplifiers are AD708, whose typical drift is 0.3μV/℃, minimal compared to platinum resistance temperature sensor sensitivity of 10mV / ℃, even if the ambient temperature is 20 ℃, it has only 0.3μV / ℃ ×20 ℃ = 6μV error.
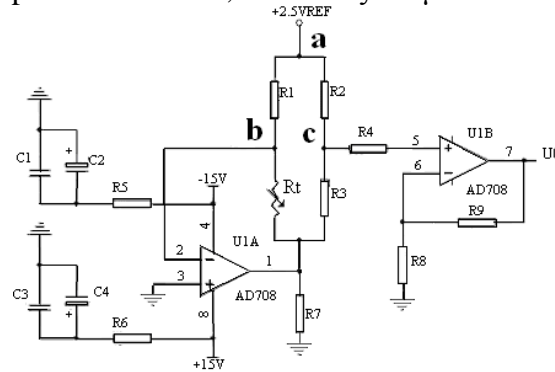

Fig. 4 Testing Temperature Schematic Circuit Diagram

By using circuit diagram shown in Fig. 4, the output of voltage and temperature equation is Uout = -2.938+0.06375T, namely, the temperature changes by 1 ℃, the output voltage of circuit varies 0.06375V; the data acquisition is achieved by using a 14 A/D card, with a resolution of P＝5V/214＝0.000305 (V), and thus the temperature resolution of the temperature measuring circuit is P/0.06375 = 0.005 ℃.

Temperature Compensation Model. Precision sampling resistor, A/D conversion chip and a reference voltage source VRef temperature drift coefficients were 5×10^{-6}, 3×10^{-6}, and 25×10^{-6}. Because the sampling resistor and A/D conversion chip temperature drift are within the accelerometer measurement accuracy to the extent permitted, a greater accelerometer output offset drift coefficient of the reference voltage VRef is too large. Within the system operating temperature range, the reference voltage change and temperature change are approximately linear.

When the temperature of the A/D converter circuit is increased, VRef decreases, the measured A/D converter chip input voltage Vi is smaller than the true value Vi, and Vi and A/D converter temperature change is in linear relationship. Therefore, when the A/D converter circuit temperature increases, the measured accelerometer output is smaller than the true input and in a linear relationship with temperature. When the A/D converter circuit temperature increases by 20℃, the reference voltage drift is 10^2 magnitude, i.e.0.0005g due to changes in the digital accelerometer output, when INS works at the room temperature, the increased temperature of A/D converter circuit is usually around 20 ℃, hence it is necessary to compensate accelerometer output error, which is caused by A/D converter circuit temperature changes before the calibration of accelerometers [5, 6].

To measure the impact of A/D converter circuit drift on the accelerometer output, the author has had a temperature test of A/D converter circuit. Test methods are as follows: put accelerometer assembly on the base, put A/D converter circuit into a temperature control box in order to measure A/D converter circuit drift effect on the accelerometer output, and conduct A/D converter circuit temperature test. Keep on for one hour, until the temperature of accelerometer and A/D circuit is stable, adjust the temperature control box to 50℃, and record the output value of accelerometer and temperature sensor. Fit the accelerometer output and temperature. Linear relationship between vertical accelerometer output and the corresponding A/D chip temperature:

$$P = 17628.66 + 0.4511T \tag{3}$$

Wherein, P is the vertical direction accelerometer digital output and its variation, and T is the corresponding A/D chip temperature of accelerometer.

Compensate the set of measurements. Table 1 shows the accelerometer output error before and after the compensation; after the compensating, the accelerometer reading has met accuracy requirements of accelerometer measurement accuracy, where data acquisition accuracy is better than5×10^{-5} g.

Table 1 Accelerometer Output Error before and after Compensation

	Accelerometer Output Error	
	Before Compensation	After Compensation
X Accelerometer	1.22×10^{-4}	3.84×10^{-5}
Y Accelerometer	9.01×10^{-5}	2.22×10^{-5}
Z Accelerometer	1.13×10^{-4}	3.37×10^{-5}

Conclusion

(1) The high-resolution A/D converter chip can achieve the conversion of the accelerometer signal.

(2) Due to its accuracy's vulnerability to temperature drift, linearity and other factors, the system must use the A/D converter chip output; after compensating for temperature drift, accelerometer output accuracy has been significantly improved.

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