Design and FPGA Implementation of High-speed Parallel FIR Filters

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Abstract: This paper proposes a novel design method of parallel Finite Impulse Response (FIR) filter, which structure is parallel transposed. It can increase the running speed by *M* times compared with the serial FIR filter, where the *M* is the number of sub-filters, and the parallel FIR filter only introduces very small delay. Firstly the theoretical foundation of parallel FIR filters is analyzed. An example of the floating point parallel transposed FIR band-pass filter is given to verify the algorithm. Then a parallel transposed FIR band-pass filter is designed, which has optimum fixed point coefficients. Finally the fixed point of this filter is implemented in Xilinx's Virtex-6 Field Programmable Gate Array (FPGA). According to the simulation results, this filter has smaller resource consumption and its sampling rate up to 1.2GHz.

Introduction

Finite Impulse Response (FIR) filters are of great importance in digital signal processing (DSP). Their characteristics of linear phase and unconditional stable make it very useful for building high stable performance filters [1]. Nyquist sampling theorem states that the sampling rate of the digital filter is at least twice the bandwidth of the highest signal [2]. In some high-speed wideband communication system, e.g. high-speed broadband satellite receiver, the transmission data rate is getting higher and higher, so the FIR filter operation speed requirements are also increasing, more than 1GHz. This raises demanding requirements of the hardware implementation for FIR filter [3].

With the continuous development of science and technology, FPGA's internal logic resources has become increasingly diverse, its structure flexibility and re-configurability become the preferred solution of many high-performance applications [4]. The computational speed of Xilinx Virtex-7 up to 740MHz [5]. But if using serial methods, FPGAs can't achieve the FIR filter whose sample rate over 1GHz, so the filter's implementation structure must be improved. We can use parallel processing to reduce the speed requirements of the chip, so that it can be implemented in FPGAs.

In recent years, fast parallel filter structures have been widespread discussed. The optimization method of the fixed-coefficient FIR filter is discussed in [6]. In this method, the filters coefficient is decomposed into a power of 2, to reduce the computational complexity of the FIR filter, thereby improving the operation speed of the filter. The matrix form of linear convolution is used in [7, 8]. In these structures, the delay elements are regularly placed and the fast linear convolution algorithm can be used to reduce the hardware cost, especially the number of multiplications. Conway et al. [9] proposed a method based on two-stage sub-filters to reduce the resources of the filters, which requires large number of delay elements and adders.

This paper proposes a novel design method of parallel FIR filter, which structure is parallel transposed. Such filters have a simple structure and small delays. It is very suitable for the implementation of short order FIR filters. This paper describes the theory of the FIR filters, and gives an example FIR filter used in the paper which includes the structure of parallel transposed FIR filter and the floating-point simulation results.

Parallel transposed FIR filter

Theory of Parallel transposed FIR Filter. Assume the input signal of digital filter is $x(n)$, the output signal is $y(n)$, then the mathematical expression of FIR filter can be expressed as [10]:

$$y(n)=\sum_{k=0}^{N-1}h(k)x(n-k) \tag{1}$$

where the $h(k)$ (k=0, 1, ⋯, N-1), is the impulse response coefficients of the FIR filter, N is the length of the filter (i.e., order of the filter). It uses a non-recursive form to describe FIR filter.

Frequency response of the FIR filter can be expressed as:

$$H(z)=\sum_{k=0}^{N-1}h(k)z^{-k} \tag{2}$$

Eq. 2 provided a analysis method of filters. The *Signal Flow Diagram*(*SFG*) of the transposed FIR filter can be derived by direct form. The derivation of 4-tap transposed FIR filter as shown in Fig. 1.

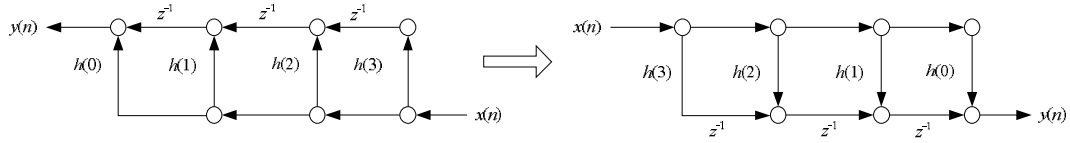

Fig. 1 *The derivation of 4-tap transposed FIR filter*

According to Fig.1, we can derive the block diagram of 4-tap transposed FIR filter, shown in Fig.2.

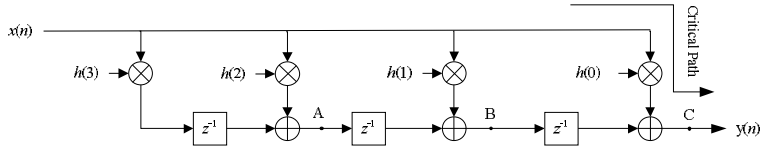

Fig. 2 *The block diagram of 4-tap transposed FIR filter*

As can be seen from Fig.2, the input data $x(n)$ simultaneously broadcast to all of the multipliers, which makes all of the multiplication can be completed in one clock. Compared with the structure of the direct form FIR filter, its critical path, determined by the computing time of a multiplication and an addition operation, has been shortened. Therefore, the sampling period of this structure can be expressed as:

$$T_S \geq T_{Multi}+T_{Add} \tag{3}$$

Correspondingly, the sampling rate of this system is:

$$f_S \leq \frac{1}{T_{Multi}+T_{Add}} \tag{4}$$

Structure of Parallel transposed FIR Filter. Unfold transform is a main operation of the serial FIR filter to parallel. The diagram of 4-Unfolded of 4-tap transposed FIR filter as shown in Fig. 3. Serial transposed FIR filter is a *single-input single-output* (SISO) system and parallel transposed FIR filter is a *multiple-input multiple-output* (MIMO) system. Each clock cycle, there are four parallel input signal, its corresponding input / output equation can be expressed as:

$$\begin{aligned}
y(4k)&=x(4k)h(0)+x(4k-1)h(1)+x(4k-2)h(2)+x(4k-3)h(3)\\
y(4k+1)&=x(4k+1)h(0)+x(4k)h(1)+x(4k-1)h(2)+x(4k-2)h(3)\\
y(4k+2)&=x(4k+2)h(0)+x(4k+1)h(1)+x(4k)h(2)+x(4k-1)h(3)\\
y(4k+3)&=x(4k+3)h(0)+x(4k+2)h(1)+x(4k+1)h(2)+x(4k)h(3)
\end{aligned} \tag{5}$$

For k is the number of clock cycles. From the Eq. 5, in the kth clock cycle, there are four inputs $x(4k)$, $x(4k+1)$, $x(4k+2)$ and $x(4k+3)$ to be processed and four sampling points are generated simultaneously. In parallel processing system, the critical path is kept constant, and the system clock period (T_{clk}) must be met:

$$T_{clk} \geqslant T_{Multi}+T_{Add} \tag{6}$$

Because four sampling points are processed in a single clock cycle, so the sampling cycle of the system into the original 1/4, namely:

$$T_S=\frac{1}{4}T_{clk} \geqslant \frac{1}{4}(T_{Multi}+T_{Add}) \tag{7}$$

So, under the condition of invariable in the system clock cycles, 4-tap parallel processing can improve the system's sampling rate 4 times (i.e. system throughput increased by 4 times). This is a concrete manifestation of the resource exchange rate.

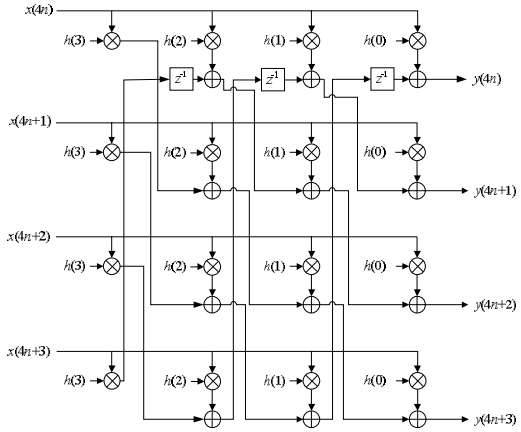

Fig. 3 *The block diagram of 4-tap parallel transposed FIR filter*

Matlab Simulation. If the system sampling rate is 1.2GHz, 3dB bandwidth is 400MHz, the upper and lower cutoff frequencies is 50MHz and 550MHz, the transition bandwidth is 50MHz, band attenuation is 60dB and band jitter is 1dB. A 49-tap parallel transposed FIR band-pass filter was designed by Matlab simulation software and its amplitude-frequency characteristics and phase-frequency characteristic curve as shown in Fig. 4. From the figure, we can see that the filter frequency response characteristics meet the system design requirements, and in the pass band, the phase response of the filter meets the linear phase, which can be further reduced the phase distortion introduced by the filter output on the system.

Do the fixed-point simulation for FIR filter, the purpose is to pave the way for the subsequent filter realization on FPGA. The floating-point coefficients of FIR filter is converted to 12-bit fixed-point, and its simulation results as shown in Fig. 5. The length of the fixed-point coefficients, impact on the pass-band frequency response characteristic, is not obvious. Its mainly affects the stop-band characteristics. In addition, the phase response in the pass-band is still linear.

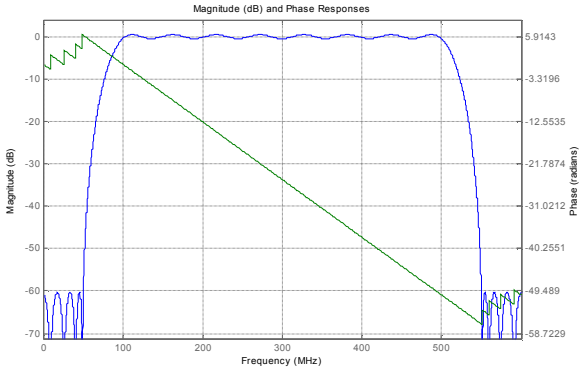

Fig. 4 *The amplitude-frequency and phase frequency curve of 49-tap FIR filter*

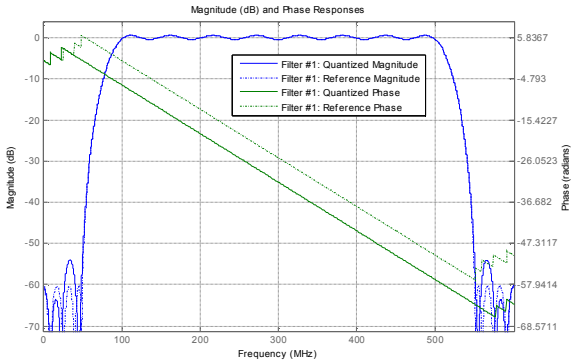

Fig. 5 *The fixed-point simulation of 49-tap parallel transposed FIR band-pass filter*

Design and implementation of 49-tap parallel transposed FIR band-pass filter

Implementation structure of 49-tap parallel transposed FIR band-pass filter. The implementation structure diagram of 49-tap parallel transposed FIR band-pass filter as shown in Fig. 6. The 49-tap parallel transposed FIR band-pass filter was implemented in Verilog HDL, and simulated using Modelsim10.0c.

FPGA implementation and verification. The Modelsim simulation results combined with Matlab as shown in Fig. 7. We can see from the Co-simulation results that the behavioral simulation output result was fully consistent with the HDL simulation output, and the statistical results of error bits were 0 bit. We presented the real hardware implementation on the Xilinx Virtex-6 XC6VLX240T FPGA.

Although the highest operated rate of Virtex-6 family chips is higher than 600MHz , the required rate of the filter is 1200MHz, if the filter is divided into 4-Parallel groups; the clock frequency of data in each channel is 300MHz after being decelerated, wherein FPGA can be easily realized.

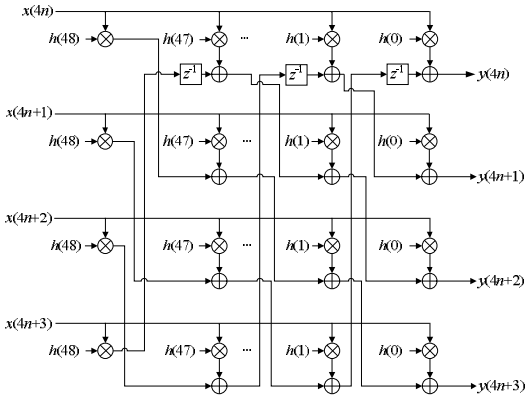

Fig. 6 *The implementation structure diagram of 49-tap parallel transposed FIR band-pass filter*

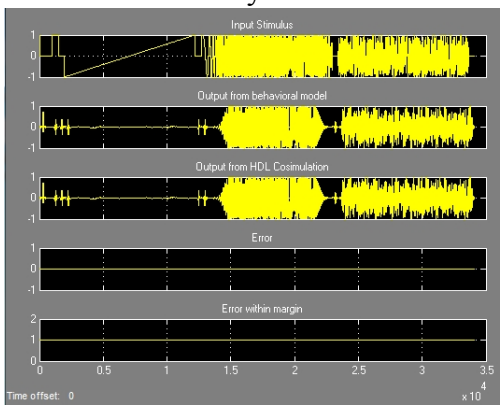

Fig. 7 *The Modelsim simulation results combined with Matlab*

Summary

We have implemented the 49-tap parallel transposed FIR band-pass filter in Verilog HDL, and simulated using Modelsim10.0c. The architecture of 4-Parallel filter was based on transposed filters. The final results indicate that it can efficiently increase the equivalent rate of the filter and implement high-speed filtering, which cannot be achieved by the traditional serial filter, though this structure has great resource consumption. Because of its highest equivalent rate of this filter (up to 1200MHz) and the simple structure, the parallel filter can be widely applied to various occasions where high-speed digital filters are needed.

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