Design of analog acquisition and storage system about airborne flight data recorder

Changyou Li[1, a], Pengfei Sun[1, b *]

Mechanical and Power Engineering College, Henan Polytechnic University, Jiaozuo 454003, China

[a]LCY@hpu.edu.cn, [b]453651337@qq.com

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Abstract. In view of the problem that the increasing complexity and storage capacity about current flight parameters, proposed a design program of analog data acquisition and storage system about airborne flight data recorder based on STM32. Adopting STM32F103ZET6 as the master controller to c analog and store it to the SD card in a certain frame format. USB data uninstall interface is used to communication with the host PC, so as to uninstall and analysis the data in the SD card. Experiments show that the system has improved the way of flight data acquisition, storage and uninstalling, and it also has the advantages of high reading and writing speed, plugging convenient, low-power consumption and high reliability. It has a strong theoretical and practical value.

Introduction

Airborne flight data recorder mainly completes the task of acquisition and storage flight data[1]. The airborne flight finishes recording the flight data with tape in early stage, but this way has the shortcomings such as recorded fewer parameters, big errors and so on. So, at the late eighties, we gradually began to use the disk and solid state recorder to record flight data that acquisition. Due to the rapid transmission and strong real-time of analog data in the aircraft during flight, Therefore, it has a high value to design a new airborne flight data recorder system to achieve the function of acquisition and storage the analog data real-time and high speed.

System working principle

The STM32F103ZET6 microprocessor integrates 64K bytes of SRAM and 512K bytes FLASH[2]. It Has a rich of I/O and peripheral resources, high computing speed, low cost, small size and many other advantages. Its working clock is up to 72MHz so as to a high data processing and program execution speed. Therefore, this design uses STM32F103ZET6 as the main control center.

This paper designs a corresponding signal conditioning circuit aiming at the characteristics of analog signal. By filtering, amplification and shaping treatment for the analog to meet the acquisition requirements, and then, the ADC of STM32F103ZET6 collects the analog signals by a certain order and frequency based on presetting program instruction. The timer module is responsible for setting the acquisition frequency ADC[3]. Signal storage module adopts SD card as recording media, STM32F103ZET6 forms a packet according to a data storage format for the analog signals which collected, then, sent it to the data buffer. We write data into the SD card in a standard path when the buffer reaches to a predetermined amount. USB data uninstall interface module connects the system with the host PC directly via USB cable, its function is to uninstall the analog data at the end of flight test. The JTAG interface circuit is used to achieve the function that uses J-LINK emulator to debug and download the control program. The analog acquisition and storage system block diagram is shown in Fig.1.

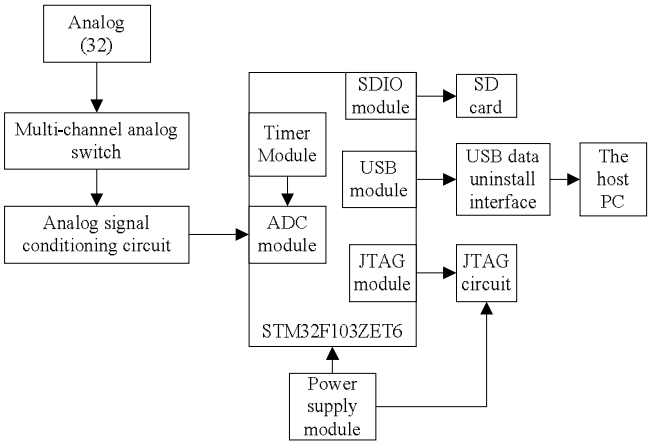


Fig.1 Analog acquisition and storage system block diagram

Hardware design of the system

The analog signal is related to the engine system, navigation system and loop attitude control system in the flight parameter signal statistics. It has a total of 32 flight parameters[4]. So, we should capture 32 analog signals one time. But the external channel which STM32F103ZET6 integration has only 16, therefore, we need use Multi-channel analog switch to achieve analog signal acquisition. Multi-channel analog switch achieves the function by switching each channel in turn, and setting the analog signal sampling interval by a timer. Analog Multiplexer ADG706 is a 16-channel analog switch. It has so many advantages such as monolithic CMOS process, 28-CDIO package, working voltage is set at ± 17V that can meet the needs of the design fully.

The analog measurement range of the airborne flight data recorder system is 0 ~ 5V, 0 ~ 10V, ± 5V and ± 10V, but the working voltage range of ADC module in STM32F103ZET6 is 2.4 ~ 3.6V. So, we add a first-order RC low-pass filter in the signal conditioning circuit to filter the sharp pulse signal which generates due to the outside interference. At the same time, we make the analog signal differential amplification by a differential scaling circuit which amplifiers by differential operational OPA4342, so as to make the analog signal into the matches signal which ADC conversion input.

The system needs to collect 32-channel analog signals. It completes the acquisition by the regular channel conversion mode of ADC which integrated in STM32F103ZET6. All devices are built around the analog-to-digital converter. The data that converted by ADC is stored into a 16-bit rules channel data register. We write it into the SRAM memory by DMA. We set a DMA requirement at the end of the analog to digital conversion. We also should set the analog watchdog. It will trigger the watchdog interrupt when the voltage of acquisition is greater than the threshold. The analog signal acquisition circuit schematic is shown in Fig.2.

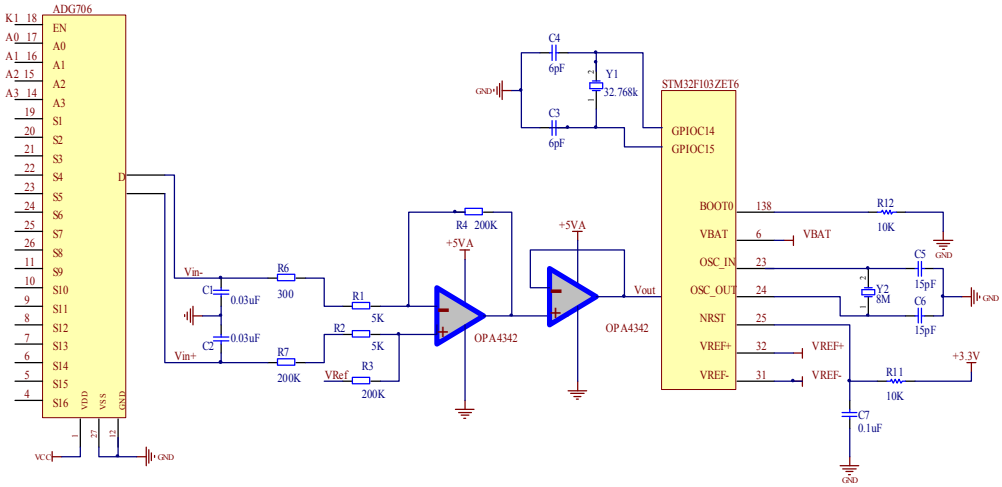


Fig.2 Analog signal acquisition circuit schematic

This design stores the analog which acquisition via driver SD memory card by the SDIO module integrated by STM32F103ZET6, so as to meet the need of high-speed storage for airborne flight data recorder[5]. So, this system is added a SD card slot for SD card installed.

The airborne flight data recorder began to enter the ground read mode when the flight is over. Then, we need uninstall the analog data which stores in the SD card. This system uses USB data uninstall interface to uninstall analog data from SD card to PC and completes the task of analysis data with the PC program based on the Windows operating system[6]. USB data uninstall interface circuit schematic is shown in Fig3. Pin 1 is connected to 5V, and the power is supplied by the PC port. 2 and 3 pin is used to connect with the data lines. The shell is connected with pin 5 to ground. The resistance has an effect on cushion protective during the data transfer process. We elect 22Ω as the resistance. The capacitor and resistor in the circuit have the effect of filtering, so as to improving the quality of data transmission.

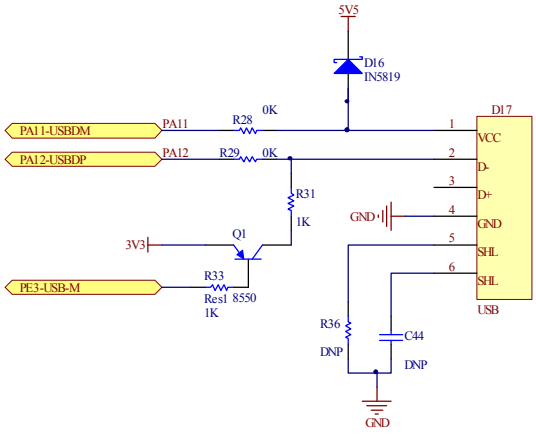


Fig.3 USB interface circuit principle schematic

Software design of the system

According to functional specifications and technical requirements, we conduct a software design. It achieves the function of the power to identify, resource initialization, system configuration, data acquisition and processing and so on.

We adopt DMA transfer mode, so the converted data can transfer to SRAM by DMA during the analog data acquisition with ADC in STM32F103ZET6. Then, we can process the analog data. When programming, the first work is enable each port clock, then, configured GPIO which in the ADC corresponding channel as an analog input mode. We use channel 1 of DMA to transfer analog data in the ADC peripheral data register to memory, and both memory and peripheral addresses are fixed. The data size of each transfer is half-word (16). We complete the analog data transfer uninterrupted with DMA cycle transfer mode. We elect ADC_DR data register as the DMA transfer source address because of the converted analog data is stored in it.

This design uses dual AD synchronized acquisition. The ADC is configured in a certain order to scan converter for each channel due to we should make the 16-channel acquisition signal together[7]. The design adopts an external trigger mode, then, ADC starts analog to digital conversion after receiving the trigger signal. We use a right-aligned manner to store the conversion value by ADC in a 16-bit variable. The ADCCLK is configured 9MHz, ADC channel is configured for the same sampling period 55.5, then, we can get the conversion time of a channel for this experiment is 7.56s based on the formula of ADC sampling time.

It achieves the function of collecting multiple analog and decoding data according to frame synchronization and code synchronization. We encode and store the analog by the control of master module STM32F103ZET6 after acquisition. The frame format of multiple analog signal acquisition is as follow: 16 bytes of data + 2 bytes of frame count + frame end AC80.

STM32F103ZET6 microcontroller itself integrates 64K bytes of SRAM. We divide it into two spaces as the buffer space before the analog data storing in the SD card. Each of the space can store 32

* 2K bytes data. It signs as cache1 and cache2. The analog data that read by the system is stored in cache1. We start cache2 to store data when cache1 is full. At the same time, write all the analog data in cache1 to the SD card. The system adopts the program of two cache work alternating. It can not only ensure the analog data to read uninterrupted but also ensure that the data stored in the SD card stable, fast and without loss. Double ping-pong buffer flow chart is shown in Fig.4.

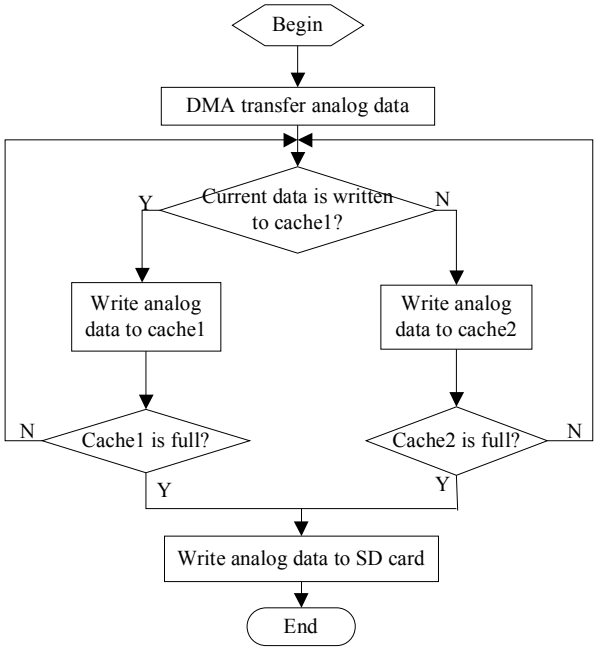


Fig.4 Double ping-pong buffer flow chart

The application program process of USB data uninstall interface is as follows: firstly, open the function of USB device by calling the corresponding function. Then, the corresponding function button start to send relevant instruction to WDM after the USB device is found. STM32F103ZET6 main control module completes the function of send data and erase and so on when the USB device receives the instruction. We read the analog data by using the function of ***ReadFile*** when the device sends out the data transmission request. After the application functionality is complete, we close the USB device and release the hardware resource by calling the ***CloseHandle*** function. USB read SD card flow chart is shown in Fig.5.

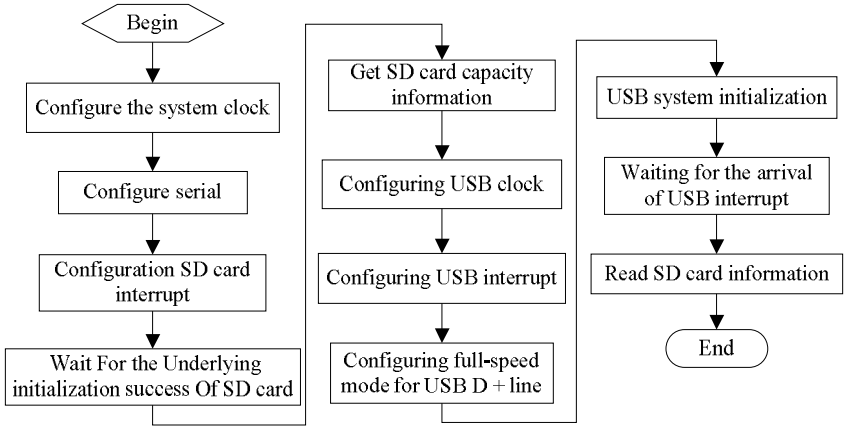


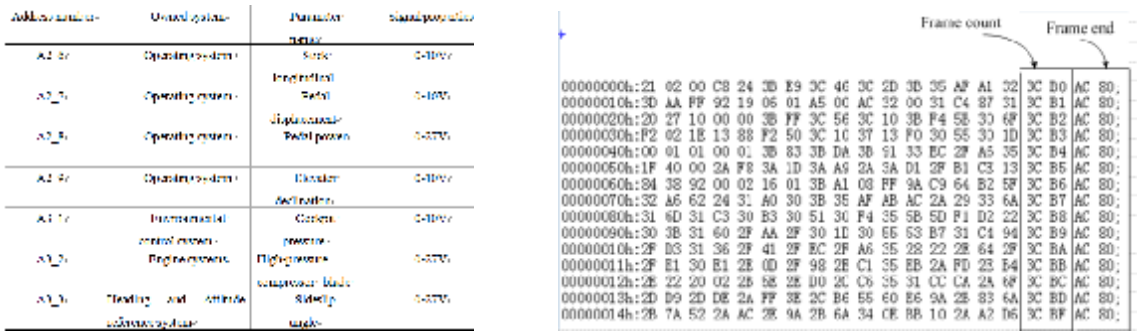
Fig.5 USB read SD card flow chart

Experiments and results

This experiment makes the test board voltage stability in 3.3V by power circuit. We select serial 1, wire JINK and the serial with STM32 test board correctly, plug the SD card, then, send the analog signal to STM32 and make the complied program download to the test board. At last, we can read the

analog data stored in the SD card by using a USB cable to connect PC and the USB data uninstall interface.

When using the USB cable to connect the USB port and PC, PC Host Test Board recognized as the USB mass storage devices, it is modeled as a U disk access, so that the application can access the local hard drive like the same access data stored in SD card data files, enabling easy switching between the PC and the test plate data. Is shown by the value of analog with the host PC, a USB connection, read, and Fig.6 (a) shows the analog part of the need to collect, and Fig.6 (b) shows the acquisition and storage of analog Fig.6 the amount saved in SD card renderings.



（a） Part of fly parameters need to collect （b） Part of acquisition data saved in SD card

Fig.6 Experiment result

Conclusion

The results show that, by making full use of the rich STM32F103ZET6 chip hardware resources and the corresponding hardware and software design, to achieve the airborne flight data recording system for fast analog signal acquisition and storage capabilities, the system can also interface with the host PC via USB machine direct connection, the data is read, and improved use of flight data acquisition and storage and unloading of the way, read and write speed, plug convenient, low power consumption, reliability, and has a strong theoretical and practical value.

Acknowledgment

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