A Low-Power Single-Stage RF Receiver Front-end: Variable Gain-controlled Double-balanced LMV Cell

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***Abstract*—This paper presents a low-power, single-stage, and variable-gain controlled double-balanced type RF receiver front-end, called DB-LMV cell, by merging low-noise amplifier (LNA), mixer, and voltage-controlled oscillator (VCO) exploiting a series *LC* (SLC) network. The low intermediate frequency (IF) or baseband signal can be directly sensed at the drain nodes of the VCO switching transistors and filtered out at the IF output port by adding a simple resistor-capacitor (*RC*) filter. Variable gain control function is achieved by adding a negative resistance cell at the IF output. Using a 65 nm CMOS technology, the proposed DB-LMV cell is designed. Oscillating at around 3.2 GHz, the phase noise of the proposed DB-LMV cell is −67.7 dBc/Hz, −91.1 dBc/Hz, and −111.8 dB/Hz at 10 kHz, 100 kHz, and 1 MHz offset frequency, respectively. The simulated voltage conversion gain varies linearly from 23 dB to 51 dB. The noise figure is about 6.3 dB at 1 MHz offset frequency. The LMV cell consumes 0.56 mW dc power from a 1 V supply.**

Keywords-CMOS; phase noise; series LC tank; LMV cell; noise figure; variable-gain; voltage-conrolled oscillator (VCO) .

I. INTRODUCTION

Low power, low-voltage, and highly integrated circuits are always the main topics for integrated circuit design, especially very important for mobile wireless communication systems due to the limitation of battery life. For highly integrated low-power receiver front-end, a current reuse technique is typically chosen across different functional blocks. A popular method is cascoding the mixer on top of the input stage of the low-noise amplifier (LNA), while less frequent is stacking mixer and voltage-controlled oscillator (VCO) [1-4]. In [1], a double balanced mixer is stacked on top of the voltage-controlled oscillator (VCO) by using the current reuse topology. The radio frequency (RF) input signal is applied to the input of the mixer, and the oscillator signal is applied to the source nodes of the mixer. Moreover, this topology applies a separate dc bias to the VCO. In [2], the RF front-end merges LNA, mixer, and VCO (LMV) in a single stage. This topology stacks VCO on top of the mixer. The current source of the mixer is modified as the LNA with inductor degeneration. This topology performs RF amplification, mixing, and local oscillator (LO) generation while sharing the same bias current and the same devices among all the blocks of the RF front-end, resulting in a very low-power and small-area chip solution.

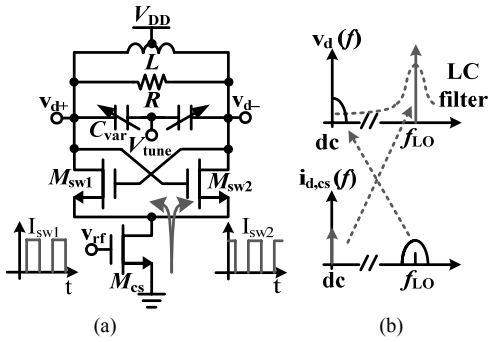

Figure 1. (a) Conventional PLC VCO as a mixer and (b) its frequency response.

Since the intermediate frequency (IF) outputs are connected to the source nodes of the VCO, the voltage gain is limited due to the low impedance at the source nodes. A conventional VCO with a current source can be considered as a mixer when an RF signal is applied to the input port of the current source. For the conventional VCO, the down-converted IF signal at the VCO output is negligible due to the low impedance at the low frequency. If a series resonator is employed, the impedance is high at the low frequency and the IF signal can be recovered without any signal loss. In this paper, a single-stage variable-gain controlled double-balanced LMV (DB-LMV) cell is proposed combining LNA, mixer, and VCO to suppress the LO leakage at the IF output. By exploiting a series *LC* (SLC) network instead of a parallel *LC* (PLC) network, the baseband or low frequency IF signal can be directly extracted from the drain outputs of the VCO.

II. PROPOSED LMV CELL DESIGN

A conventional *LC* tank oscillator, as shown in Fig. 1, performs the mixing process since an RF signal in the VCO bias current is down-converted by the switching transistors. Also, by the same mechanism, the *dc* current of M_{cs} is up-converted to the LO frequency.

With the complete switching is assumed for the M_{sw1} and M_{sw2}, the current at the VCO output port is given by

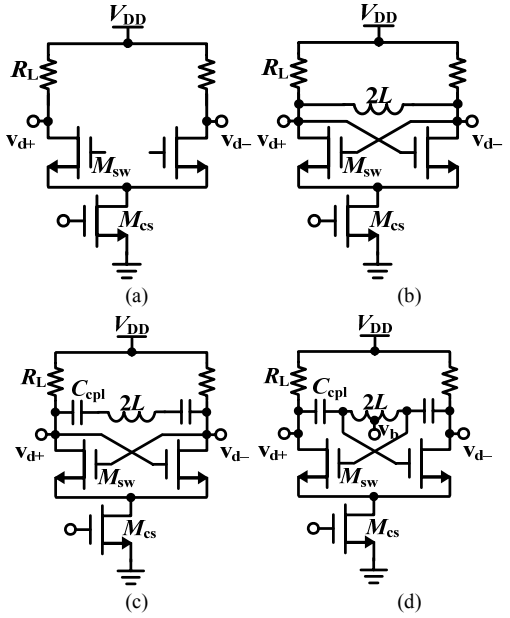

Figure 2. Several mixer topologies (a) single-balanced mixer, (b) PLC VCO as a mixer, (c) SLC VCO as a mixer, and (d) SLC VCO as a mixer with separate gate bias v_b.

$$i_O(\omega) = \frac{4I_{CS}}{\pi}\cos\omega_{LO}t + \frac{2}{\pi}g_m v_{RF}\cos(\omega_{LO} - \omega_{RF})t + \ldots \quad (1)$$

$$v_{LO}(\omega) = \frac{4I_{CS}R}{\pi} \quad (2)$$

where I_{CS} and g_m are the *dc* current and transconductance of the current source M_{cs}, respectively. The first term in (1) is the LO component of the VCO. The low frequency IF signal (the 2nd term) is severely attenuated since the inductor of the PLC tank is short at around *dc*. Also, the high frequency component (the 3rd term) is attenuated by the PLC tank. Attempting to sense the down-converted component at the VCO output unavoidably degrades the VCO phase noise [2].

One possible solution is to exploit the SLC network for the VCO to extract both LO and IF signals. Fig. 2 shows several mixer topologies. In Fig. 2 (b), the IF signal is shorted with the inductor. Fig. 2 (c) and (d) show the SLC VCO as a mixer where the coupling capacitor C_{cpl} and the inductor 2*L* form a SLC network. When an RF signal is applied to the input of the transconductance stage, the coupling capacitor C_{cpl} is open at IF frequency and they are exactly the same as the single-balanced mixer in Fig. 2 (a). Fig. 3 shows the final single-balanced LMV (SB-LMV) cell by modifying the current source as an inductive degenerated LNA and adding simple first-order *RC* low-pass. As shown in Fig. 2 (c), the capacitor C_{cpl} and the inductor 2*L* are connected in series.

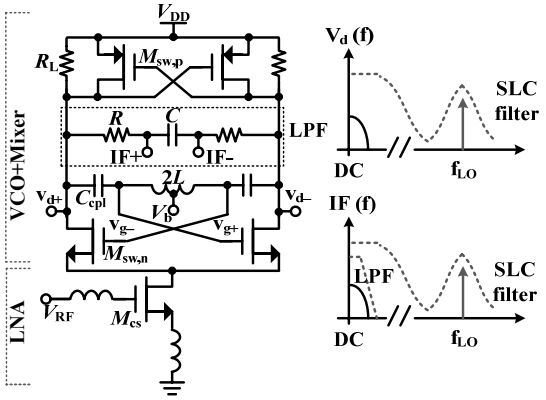

Figure 3. Finalized single-balanced LMV cell with RC low pass filter added [5].

The voltage transfer function at the connection node is given by where ω_o is the angular oscillation frequency. Considering the series loss resistance in *L*, (1) can be rewritten as

$$v_{g+} = v_{d+}\frac{\omega_o^2 LC_{cpl}}{\omega_o^2 LC_{cpl} - 1} \quad (3)$$

$$\frac{v_{g+}}{v_{d+}} = \frac{\omega_o^2 C_{cpl}R_p L}{\omega_o^2 C_{cpl}R_p L - j\omega_o L - R_p} \quad (4)$$

where R_p is an equivalent parallel resistance of inductor *L*. The voltage gain from the drain to the gate is given by

$$A_G = \left|\frac{v_{g+}}{v_{d+}}\right| = \frac{\omega_o^2 C_{cpl}L}{\sqrt{\left(\omega_o^2 C_{cpl}L - 1\right)^2 + (\omega_o L/R_p)^2}} \quad (5)$$

At oscillation frequency, (3) can be simplified as

$$A_G \approx \frac{R_p}{\omega_o L} = \frac{\omega_o L}{R_s} \quad (6)$$

From (6), it can be seen that there is voltage amplification at the connection node of the SLC resonator. This voltage amplification contributes to lower phase noise by preventing the switching transistors of the VCO core from entering the triode region [6]. The *RC* low-pass filter is designed to attenuate the VCO output component at the drain nodes while somewhat degrading the phase noise performance. The transistor M_{cs} acts as an LNA at RF, while providing the dc bias current to the VCO. Similarly, $M_{sw,n}$ performs the mixing operation while contributing the negative resistance to the VCO. Furthermore, $M_{sw,p}$ adds more negative resistance to the VCO core.

As shown in Fig. 3, RF component is down-converted around dc, and the dc component is up-converted to the LO frequency. Looking at the gate nodes, the IF component at the gate nodes is severely attenuated since the inductor is short at the IF frequency. However, looking at the drain

nodes, the IF component appears without attenuation since the C_{cpl} is open at around dc.

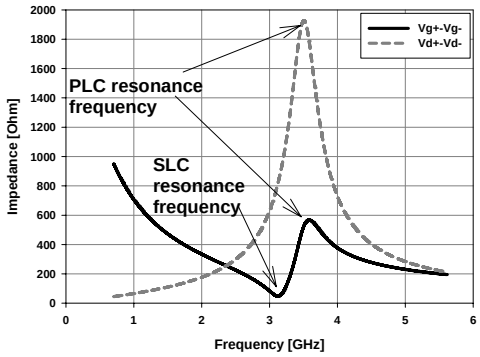

Figure 4. Impedances of the SB-LMV cell looking at the gate and drain nodes.

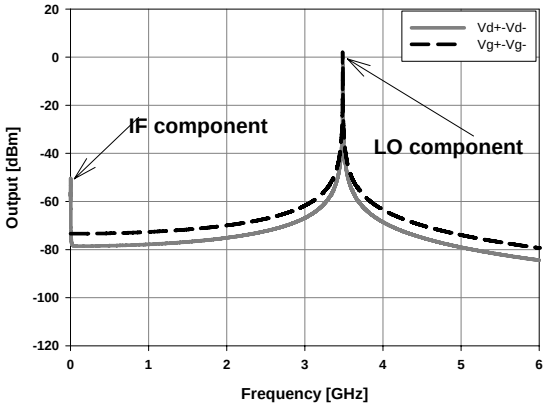

Figure 5. Output spectrum of the SB-LMV cell looking at the gate and drain nodes.

With just adding the simple *RC* low-pass filter (LPF), the LO component can be rejected with significant attenuation and leaving the down-converted signal at the IF output.

The proposed LMV cell requires only small size capacitance compared to the LMV cell in [2] which requires quite large size capacitance for the same LPF corner frequency since the impedance looking at the source nodes at the IF outputs is quite low. Fig. 4 shows the impedances and the output spectrum looking at the gate and drain of the switching transistors, respectively. As shown in Fig. 4(a), the coupling capacitor C_{cpl} can be chosen for the SLC resonance frequency to be close to the PLC resonance frequency at which the VCO phase noise is minimized [5]. Since the coupling capacitor is just short at the oscillation frequency, the final VCO oscillation frequency is finally determined by the PLC resonator composed of 2*L* and parasitic capacitances at the gate nodes in Fig. 3.

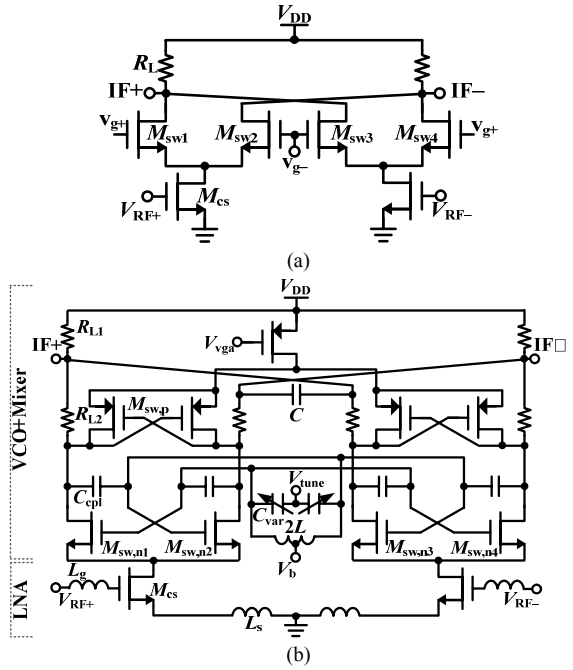

Figure 6. (a) Double-balanced mixer and (b) proposed double-balanced LMV cell.

Fig. 5 shows the output spectrum at the gate and drain nodes. As shown in Fig. 5, the IF component is severely attenuated at the gate nodes, but appears at the drain nodes without attenuation. Fig. 6 shows the conventional double-balanced mixer and the proposed double-balanced LMV (DB-LMV) cell by combining two SB-LMV cells. For the double-balanced mixer, the IF output from the drain of M_{sw1} and M_{sw3} is directly combined. However, for the double-balanced LMV cell, the IF output from the drain of $M_{sw,n1}$ and $M_{sw,n3}$ is indirectly combined through the resistor R_{L2} to keep the oscillation of the LMV cell (the outputs LO+ and LO− would be shorted without the resistor R_{L2}). The inductor is shared between two SB-LMV cells. Compared to the SB-LMV, a capacitor can be added at the IF output in the DB-LMV and its value can be minimized just to reject the higher order harmonic frequencies at the IF output. The differential IF output voltage is given by

$$V_{IF} = \frac{4}{\pi} g_m v_{RF} R_{L1}. \tag{7}$$

III. Performance of the Proposed DB-LMV Cell

To verify the performance of the proposed LMV cell, it is designed and simulated using a TSMC 65 nm CMOS technology. A symmetric inductor is used to have a higher quality (Q) factor to have a better phase noise performance. For the proposed DB-LMV cell, the dc bias current is set to have around 0.56 mA from 1 V supply voltage. The ac coupling capacitor C_{cpl} is implemented with metal-insulator-

metal (MIM) capacitor. The tuning range is varied with the MOS varactors. The RF input port is matched to 50 Ω with the input reflection coefficient of less than −10 dB.

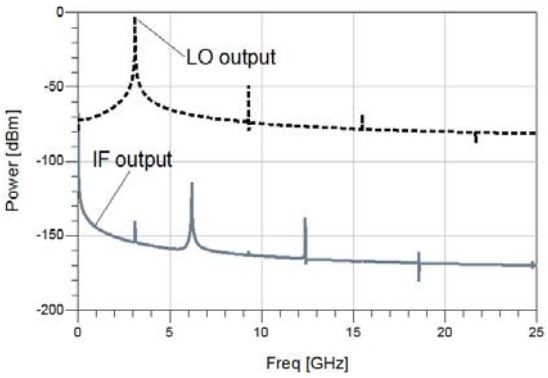

Figure 7. Simulated output spectrum at the LO and IF outputs. The applied RF input power is −100 dBm.

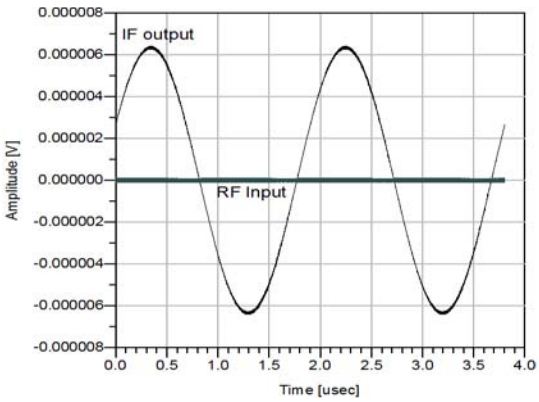

Figure 8. Voltage swing at the RF input and IF output. The applied RF input power is −100 dBm.

Fig. 7 shows the transient simulation results at LO and IF outputs. The LMV oscillates at around 3.2 GHz. As shown in Fig. 7(b), LO frequency at the IF output is severely suppressed. Higher harmonic components are also suppressed with the *RC* low-pass filter. Fig. 8 shows the signal swing at the RF input and IF output. A clean IF signal is extracted at the IF output without LO leakage. As shown in Fig. 9, the voltage conversion gain varies linearly from 23 dB to 51 dB. Fig. 10 shows the phase noise performance of the proposed double-balanced LMV cell.

The proposed LMV cell has the phase noise of −67.7 dBc/Hz, −91.1 dBc/Hz, and −111.8 dB/Hz at 10 kHz, 100 kHz, and 1 MHz offset frequency, respectively. Fig. 11 shows the simulated overall noise figure (NF) of the DB-LMV cell. The double sideband (DSB) NF is about 6.3 dB at 1 MHz offset frequency.

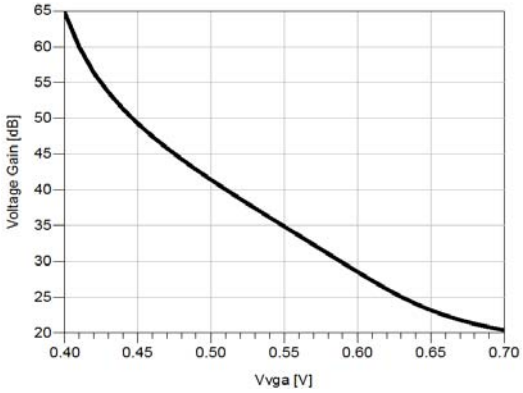

Figure 9. Voltage conversion gain of the proposed DB-LMV cell.

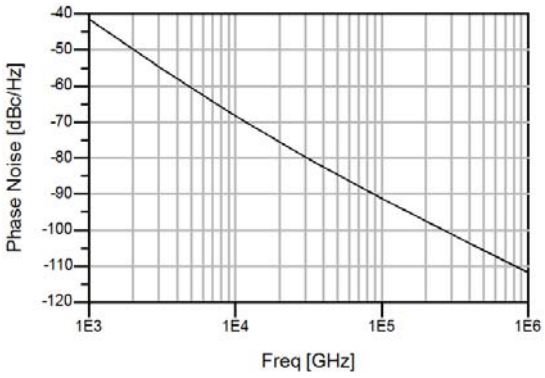

Figure 10. Phase noise of the proposed DB-LMV cell.

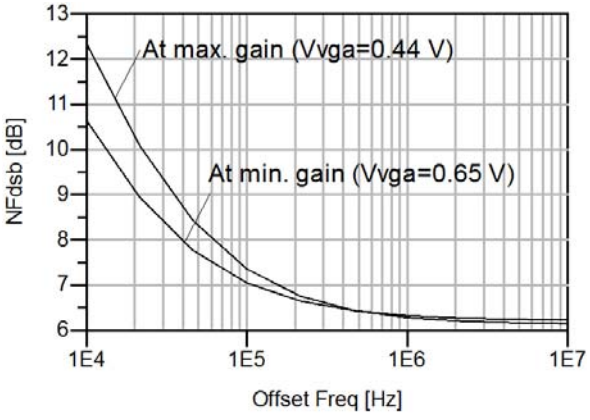

Figure 11. Simulated noise figure of the DB-LMV cell.

As shown in Fig. 11, the noise performance at low offset frequency is somewhat deteriorated since more flicker noise is directly translated to the output from the PMOS switching

core with the increased current. The frequency tuning range is from 3.15 GHz to 3.37 GHz. From the simulation results, the proposed DB-LMV cell is expected to be successfully integrated for the direct conversion receiver such as Global Positioning System (GPS), satellite communication receiver set-top box, medical applications, etc while consuming low power with just one integrated block.

IV. CONCLUSION

By utilizing a series *LC* resonator, this paper proposes a fully integrated DB-LMV cell by merging RF front-end LNA, mixer, and VCO. The proposed DB-LMV cell is designed and simulated using 65 nm TSMC CMOS technology. Operating at around 3.2 GHz, the simulation results show that the proposed DB-LMV cell achieves the phase noise of −67.7 dBc/Hz, −91.1 dBc/Hz, and −111.8 dB/Hz at 10 kHz, 100 kHz, and 1 MHz offset frequency, respectively. The voltage conversion gain varies linearly from 23 dB to 51 dB. The double sideband noise figure is about 6.3 dB at 1 MHz offset frequency. The power consumption is about 0.56 mW from 1 V *dc* supply. The proposed DB-LMV cell can be easily integrated on a chip, and applied for low-power high-performance direct conversion RF front-end receiver.

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