Design Phase Locked Loop Accuracy towards Femtosecond Magnitude

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Keywords: Wireless; Circuit; Design

Abstract. This paper studies the frequency synthesis for precision time protocol clock generation circuit, and more particularly focused on a multi-rate phase locked loop structure for generating an output signal at a desired frequency with reduced jitter towards the magnitude of femtosecond. We proposed a unique structured model that makes use of a multiple rate digital filter to match the noise spectrum characteristics of both input digital controlled oscillator reference and output voltage controlled oscillator respectively. The simulation for two rate case is carried out. This concept can be extended to more than two rates to match with additional noise sources' spectrum from the other devices such as fractional divider, etc.

Introduction

There is an increasing need for highly accurate stable clock sources to drive modern digital positioning electronics equipment, especially in the telecommunications related sector. For example, the new LTE-A (Long Term Evolution Advanced) Release 11 standard for high speed train mobile relaying requires clock sources operating at a frequency in the order of 100MHz with a jitter of 100 femtoseconds, and a wander of 16ppb (160ns). Jitter and wander are defined respectively as the short-term and the long-term variations of the significant instants of a digital signal from their ideal positions in time. This paper focuses on the jitter improvement. The common way of generating the clock at desired frequency is to derive it from a lower stable frequency source, such as a very stable crystal oscillator, using a Phase Locked Loop (PLL) with a frequency divider in the feedback path. The frequency divider can be integer-based, in which case the output frequency is an integer multiple of the source frequency; or Fractional if necessary.

One problem with this approach is that the various components within the phase-locked loop introduce noise that manifests itself as jitter or rapid fluctuations in the output signal. Various attempts have been made to solve this pressed engineering problem. One early approach was described in paper [1]. This paper described a technique employing a simple Digital Signal Processor (DSP) in the loop filter to increase the loop gain and to minimize the jitter with the same die size for the chip. The technique works reasonably well when chip size is not too small. However, at small die sizes, it eventually suffers from interference between analogue and digital circuits on the same die. Another approach is described in [6]. This patent employs a high-order steep analog filter to reduce noise, which also increases the manufacture cost. The high order or steep analogue loop further has a stability issue that is sensitive to its individual analogue parameters. Yet another solution was described in paper [2]. In that approach, the overall gain is increased through the use of dual loops, which implies that the cost may be doubled as well. The paper [4], published on IEEE MTT-S International 2012, describes a PLL with a series of Phase/Frequency Detectors (PFDs) and loop filters arranged in parallel, with each PFD-loop filter combination providing a separate input to the Voltage Controlled Oscillator (VCO) of the phase locked loop. The phase comparison of each PFD is time-shifted to avoid noise correlation. However, the last approach is limited by the correlation length, which limits noise removal to a specific reference band.

Based on above observations, we have combined the advantages of these four approaches, coming up with our own unique structure: where two phase/frequency detectors and one multiple

rate digital filter are used; similar to SiLabs digital loop, but employing multi-rate, instead of the single rate; similar to Hittite's high order filter, but done in the digital domain; similar to TI's double loop, but used only one loop; similar to Mitsubishi's homogeneous PFDs, but designed on heterogeneous PFDs.

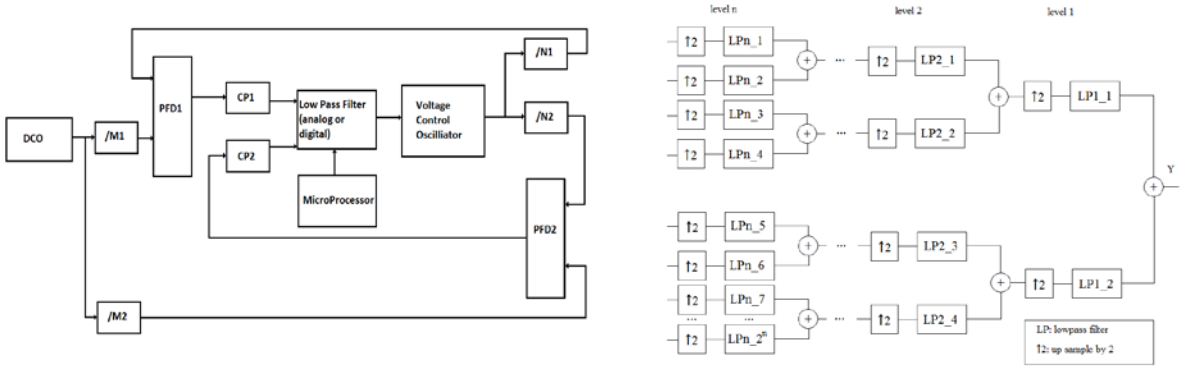
In order to reduce output clock signal's jitter, we have to pay attention to every noise source, including the voltage-controlled oscillator, Loop Filter (LF), Charge Pump (CP), various dividers, and phase/frequency detector as well. The role of the PFD is to compare the feedback signal with the reference signal in order to generate an error signal, which is used to generate a control signal for the VCO. The PFD is a low cost half-digital, half-analogue component that occupies little die space and the device itself generates little noise. However, due to its dynamic non-linearity about the origin, it will mix the noises from the other sources and create dynamic sub-harmonics or spread-spectrum noise like beating noise, which are very hard to be filtered out by traditional analogue filter. Our multi-rate approach isolates the phase/frequency detector (PFD) signal in the phase locked loop at the beginning of the signal chain to render it immune to the noise further down the signal chain.

If the jitter is required to be less than 100 fs, when the phase detector works on a 10 ns (100Mhz) cycle, there are almost 5 orders of magnitude difference, which is equivalent to maximum +50dB to -50dB open loop gain within the linear phase noise model. Typical American style Fractional architecture relies on a dual path charge pump and internal filter to increase the gain to +40dB inside the loop bandwidth. And typical European style Integer architecture uses the firmware controlled external loop filter to bring the noise down to -40dB outside the loop bandwidth. Here we use multi-rate digital filter to bring up and down the loop gain to +/-50dB, inside/outside the band.

In addition, to deal with the noises, more than two of PFDs can be ganged at different reference rates, such that the low-pass filter and high-pass filter components are separately controlled by additional loop parameters, thus making an equivalent high order filter with more tuning parameters than traditional PLL structure.

Design of the Multiple Rate PLL

The design will now be described in more detail with reference to the accompanying figures, in which: Figure 1 is a block diagram of a high gain low jitter PLL with a multiple rate digital loop filter. The phase locked loop frequency synthesizer shown in Figure 1 (a) comprises a stable crystal oscillator, for example designed to run at 40 MHz, driving a reference Digital Controlled Oscillator (DCO), which synthesize the output frequency of the crystal oscillator by an integer or Fractional value M1 and M2.



(a) PLL (b) DSP

Fig.1. Block diagram of a high gain low jitter PLL with multiple PFDs

The output of the DCO is input to the reference input of phase/frequency detection module, followed by a digital loop filter shown in Figure 1 (b). The outputs of the PFD modules are passed through a two-rate loop filter, which generates the control signal for voltage controlled oscillator. This in turn generates the output clock at the desired center frequency selected by the user depending on the average values of dividers M and N.

The output of the VCO is the feedback to the feedback input of the PFD module via two

feedback dividers, which, in this design, divides output frequency by an integer or Fractional value N1 and N2. And M1, M2, N1, N2 are all controlled by microprocessor, according to the desired output frequency. Generally, the overall gain of the phase locked loop is given by the expression:

$$\text{TotalGain} = K_{det} \times K_{VCO} \times K_{loop}/N \qquad (1)$$

Where K_{det}, K_{VCO}, and K_{loop} are the gains of the PFD, VCO, and loop filter respectively, and N is the average division integer in the feedback loop. It is noted that the total gain of the loop changes with frequency (changes with N1/N2). For any particular phase locked loop there is an optimum gain at which all the noises (from every source) are balanced and the total noise is minimized. The object of the microprocessor shown in Figure 1 is to keep the gain at the optimum value, or at least within a given range, despite fine steps in output frequency. As the output frequency is increased, the gain is reduced by decreasing the pulse width of the PFD block and vice versa. Exemplary values are K_{VCO} = 40MHz/Volt, N = 10/20, K_{det} = 10 mA/Hz, K_{loop} = 100ohm.

The adaptive selection can alternatively be implemented in pure analogue hardware, although the use of the microprocessor [3] controlled digital offers more flexibility. The selection policy depends mainly on the center frequency. Each time a new center frequency is selected by the user, the adaptive selector preferably changes the parameters of the digital filter. Its main objective is to find an optimum gain for each center frequency with the best noise separation capability. Here is the pseudo control code for the embedded microprocessor:

1. *Initialize the C/C++ code*
2. *Pick PLL mode integer Case 3.1 or else Case 3.2.*
3. *Case 3.1: Calculate DCO output frequency*
   Case 3.2: Calculate Fractional feedback division
4. *Calculate the average multi-rate loop gain*
5. *Calculate the estimated output clock jitter*
6. *If it doesn't meets IEEE1588 requirement go to step 2*
7. *Program the PLL, and adjust the Kalman filter*
8. *Check if the clock meet ITU-TG.8261 wander requirement*
9. *If yes, wait a fixed period, if no, go to step 7*
10. *Go back to step 8.*

The use of additional PFD increases the signal level at the output of the PFD module. Since the PFD module produces a relatively clean signal, the signal-to-noise ratio in relation to the noise generated in other downstream components, such as the thermal noise coming from resistive elements, or the other noise from the digital loop filter is improved.

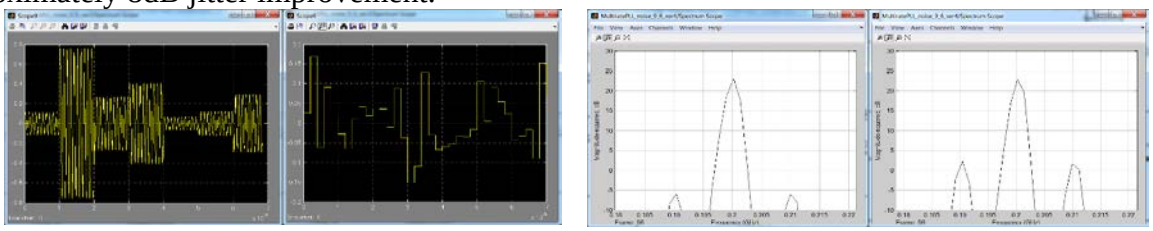
This arrangement is based on the observation that a single PFD cannot be optimized for all user selected integer or fractional center frequencies. By multiple PFDs running at different rates, they can be optimized for different frequencies. A digital signal processing engine is used to compensate temperature variation of VCO, and also to compensate for nonlinear mismatch of PFD gain. The theory is based on the fact that in a traditional single PFD PLL, the high pass and low pass filter curves are related by the equation:

$$H_H + H_L = 1 \qquad (2)$$

Where $H_H = 1/(1+T)$ and $H_L = T/(1+T)$, and T is the total open loop gain. For our compound structure shown in Figure 1, $H_H = 1/(1+\Sigma T_i)$, for each individual path, $H_{Li} = T_i/(1+\Sigma T_i)$, where T_i is its total open loop gain. The low pass filter H_L is split into two components. The individual low pass filter is no longer constrained by the high pass filter. There is now more freedom to design each filter to fit for its wide noise range. The jitter is defined as integration between 12 KHz to 20 MHz of the reference curve plus VCO curve, plus any other sources. The steeper or lower the curve in the concerned region, the smaller will be the jitter. As a rule of thumb, averagely every 6 dB drop of the curve will half the jitter number, thus a 10dB drop will result in improving from current lab test of 269 femtosecond jitter into a jitter of less than 100 femtosecond target.

The Simulation Results and Analysis

We use Matlab to simulate the performance difference of PLL with one PFD and two PFDs using digital filter. We manually add two noise sources before VCO and DCO respectively. The noise waveform we add is shown in figure 2. It turns out that our design with two PFDs enjoys an approximately 8dB jitter improvement.



(a) DCO noise (left) and VCO noise (right) (b) 2 PFDs (left) and 1 PFD (right)

Fig 2: Waveform and Spectrum Comparison

We have contributed Matlab Simulink model to Matlab file exchange server for the user community to download under BSD license. The following table shows a sample simulation result for a typical analogue RC loop filter, with R1=300 ohm, C1=250nf, C2=1nf, Kvco=140MHz/V, with the meanings of R1, C1, C3 and Kvco in accordance with standard second order RC loop filter component labels. The resistor is almost the smallest possible, while capacitors are roughly the largest possible. The resistor thermal noise for one PFD baseline case is already over 100fs. This has to be reduced first by using additional multiple rate digital filter capability. Our two rate method supports the jitter design goal of 100 femtosecond for the LTE-A Release 11, which is dedicated to high speed train base station market and allowing a low cost digital version of either Hittite's analogue PLL architecture (78fs), Texas Instrument's Dual PLL architecture (100fs) or SiLabs' digital PLL architecture (<300fs) noted above.

Conclusion

In this paper, we have discussed a phase locked loop frequency synthesizer and its Matlab model comprising: a multiple rate phase locked look. The simulation results and lab measurement show the two-rate method is promising. The future work is to extend it to three or four rate cases based on the latest quantum clock [5] available now.

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