An amplifier-sharing technique for pipeline ADCs

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Abstract. An amplifier-sharing technique for pipeline ADC is introduced, which share a common residual amplifier between two adjacent MDACs. The circuit and work principle are given in detail. Besides the amplifier-sharing, the comparators are also shared by proper clock schedule. The measurement shows that the pipeline ADC adopting this technique consumes only half of the traditional pipeline ADC.

Introduction

Analog to digital converters (ADC) is used to convert an analog signal to a series of digital codes. As the power of digital processors grows bigger and bigger, many things can be handled digitally. Despite that, the real word exists in analog form, so an ADC is needed to convert the analog signal to digital form for ever. There are many kinds of ADCs including pipeline ADC, flash ADC [1-3], fold-interpolation ADC [4-5], SAR ADC [6-7], and so on. Resolution and sampling rate are two critical specifications for ADCs. The pipeline ADC is the only architecture which can both realize high resolution and fast sampling rate.

There are many stages in a pipeline ADC, which, when working, sample and hold alternatively; that is to say, when a stage is sampling, its next and front stage is holding. For every stage, in every cycle, the incoming signal is first converted to a digital code (sub-ADC), which is then converted back to analog signal (sub-DAC), which is finally subtracted from the original incoming signal to get a residual signal, which is then amplified by an amplifier, which is so-called residual amplifier. The structure realizing sub-ADC, sub-DAC, subtraction and amplification is called MDAC. So, a pipeline ADC can be considered mainly as a series of cascaded MDACs. For traditional pipeline ADCs, every MDAC needs a residual amplifier. In this paper, we introduce a technique by which two adjacent MDACs share a common residual amplifier, and which dramatically reduce the hardware resources needed by a pipeline ADC, resulting lower power consumption.

Traditional 4-bit MDAC

Shown in figure 1 is the traditional 4-bit MDAC, which is clocked by three clocks, of which K1 and K2 are non-overlapped clocks, and K1p has the same phase relationship with K1 but with a narrow pulse. The working procedure of the traditional 4-bit MDAC is given below.

The traditional 4-bit MDAC works in cycles with each cycle being divided into sampling phase and holding phase. In sampling phase, K1 and K1p are at high level, all switches controlled by K1 and K1p are closed and the others are all opened, the incoming signal Vin is sampled on the 16 sampling equal capacitors Cs<15:0>, and the feedback capacitor Cf is reset. At the end of sampling phase, the falling edge of the K1p comes first, which makes the switch controlled by it open, resulting in the charges at the negative terminal of the amplifier being held, because there is no current leakage channel to ground for such node now. It is obvious that the sampling of the incoming signal happens at the instant of the falling edge of K1p. In order to make the sampling and comparing happens at the same time, the 16 latches are designed to at the falling edge of K1p. Immediately after the falling edge of K1p. Then, the falling edge of K1 comes, which disconnects the Vin from the sampling capacitors Cs<15:0> and cuts off Cf from ground, ending the sampling

phase. After a non-overlapped interval, the holding phase comes, with K2 changing to high level, which makes the 16 sampling capacitors Cs<15:0> either connected to REFT or to REFB, depending on the 16 outputs of the latches. The falling edge of K1 ends the sampling phase and after a non-overlapped interval, a new cycle will happen.

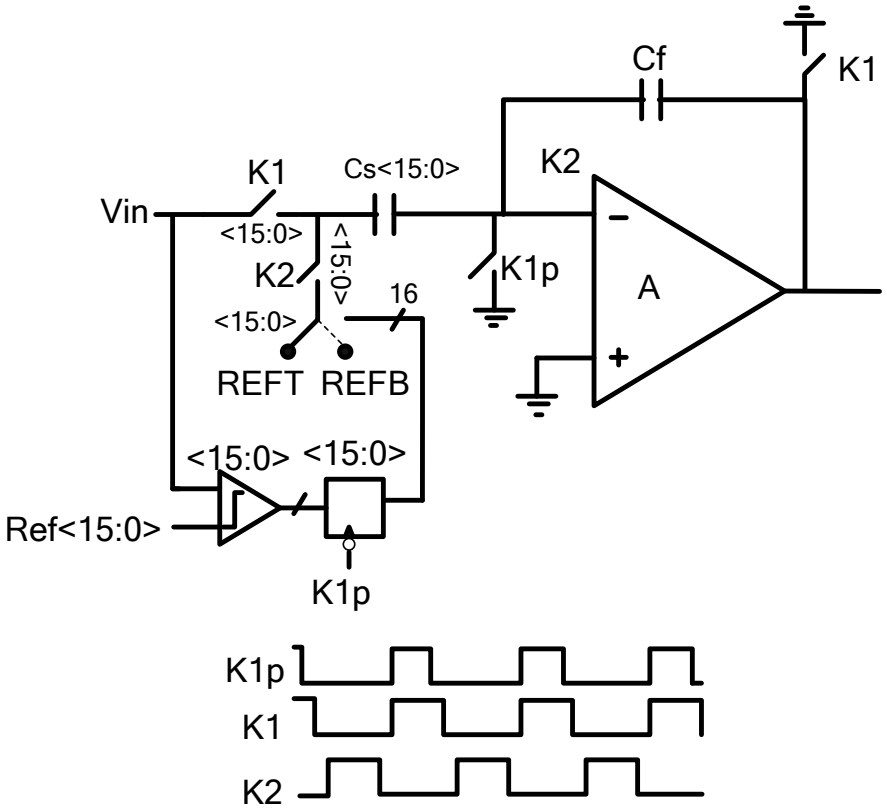

Figure 1. The traditional 4-bit MDAC.

From the analysis above, we find that the residual amplifier A is idle in sampling phase. In a pipeline ADC, cascaded MDACs sample and hold alternatively, so two adjacent MDACs may share one residual amplifier. This idea is realized by the proposed amplifier-sharing MDAC.

Proposed amplifier-sharing 4-bit MDAC

Shown in figure 2 is the proposed amplifier-sharing 4-bit MDAC, which actually consists of two cascaded traditional MDACs, In figure 2 MDAC2 reuses the residual amplifier and comparators of MDAC1. The dotted amplifier in MDAC2 doesn't exist, but a reuse of the amplifier of MDAC1. Consequently, MDAC2 is only a network of switches and capacitors without amplifier and comparators.

The work procedure of the two MDACs in figure 2 is as such: when MDAC1 is at the sampling phase without a need of residual amplifier, MDAC2 is at the holding phase, the residual amplifier being used by MDAC2; when MDAC2 is at the holding phase using the amplifier, the MDAC2 is at the sampling phase and don't need a residual amplifier.

When the pulses of K1 and K1p come, all switches controlled by K1 and K1p are closed and the others are all opened, MDAC1 gets into sampling phase and cuts off the connection from amplifier A. The Incoming signal Vin is sampled on the 16 sampling capacitors Cs1<15:0> of MDAC1, and the feedback capacitor Cf1 of MDAC1 is reset.

At the same time, MDAC2 gets into holding phase, connecting the amplifier A to its switch-capacitor network. 16 sampling capacitors Cs2<15:0> are connected either to REFT or REFB depending on the 16 outputs of the latches. The right terminal of the feedback capacitor Cf2 is connected to the output of the amplifier A, which begins to settle the output of MDAC2.

After a while, the falling edge of the K1p comes first, which makes the switch controlled by it open, resulting in the charges at the left terminal of the feedback capacitor Cf1 of MDAC1 being held. At the same time, the 16 latches of MDAC1 latch the states of the 16 comparators.

Immediately after the falling edge of K1p, the falling edge of K1 comes, which disconnects the Vin from the sampling capacitors Cs1<15:0> of MDAC1, and cuts off Cf1 from ground, ending the sampling phase of MDAC1. At the same time, the holding phase of MDAC2 ends and the amplifier A is released.

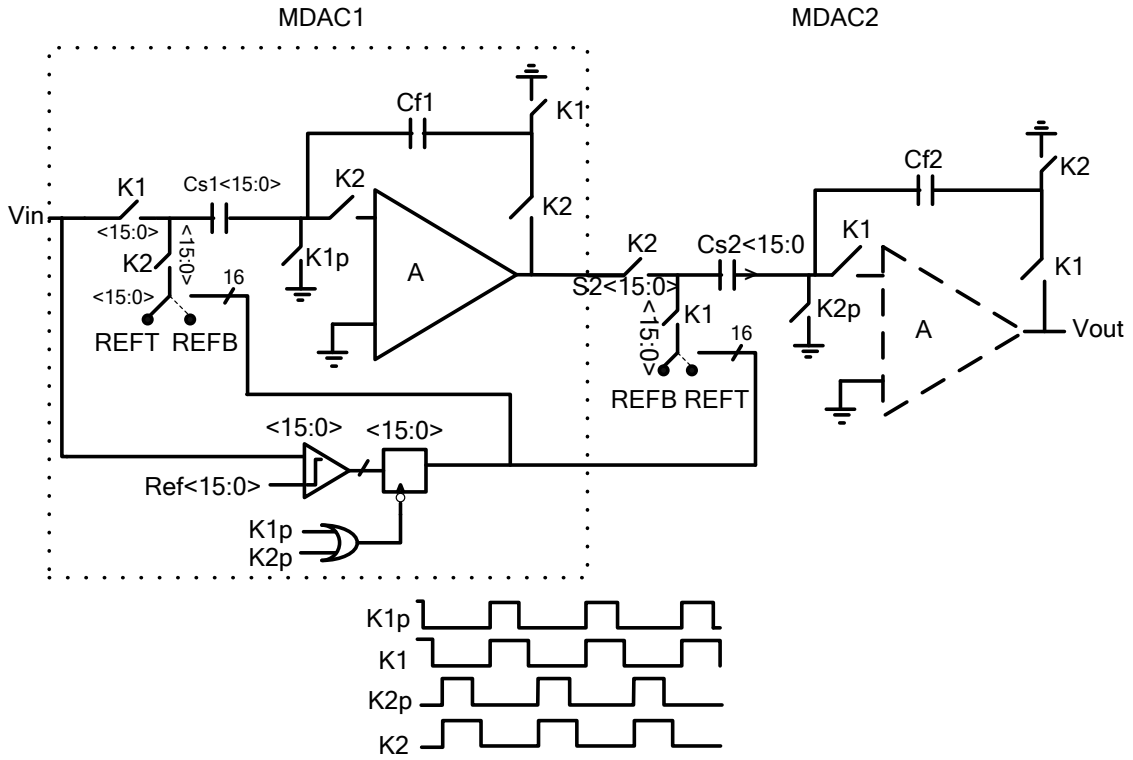

Figure 2. The proposed 4-bit MDAC.

After a non-overlapped interval, the pulse of K2 and K2p come and MDAC1 gets into holding phase, connecting the amplifier A to its switch-capacitor network. 16 sampling capacitors Cs1<15:0> are connected either to REFT or REFB depending on the 16 outputs of the latches. The right terminal of the feedback capacitor Cf1 is connected to the output of the amplifier A, which begins to settle the output of MDAC1.

At the same time, MDAC2 gets into sampling phase and cuts off the connection from amplifier A. The output of MDAC1 is sampled on the 16 sampling capacitors Cs1<15:0> of MDAC2, and the feedback capacitor Cf2 of MDAC1 is reset.

We must point out that the lathes are designed that they latch at both the falling edge of K1p and K2p, which makes the sharing of comparators possible.

Measurement

Based on the proposed amplifier-sharing 4-bit MDAC, a 14-bit pipeline ADC is constructed in a 0.18um CMOS analog/mixed signal process. Shown in figure 3 are the measured performances of the 14-bit ADC, which can sample an analog signal at a rate of 250MHz, with SNR 69dB, ENOD 11 bits, and SFDR 76dB.

Further measurement shows that the 14-bit pipeline ADC adopting the proposed amplifier-sharing technique only consumes 289mW, which is a half of the traditional one.

Conclusion

The successful application of the proposed amplifier-sharing technique in a 14-bit pipeline ADC proves that this technique can dramatically reduce the power consumption by pipeline ADC without the performance degeneration.

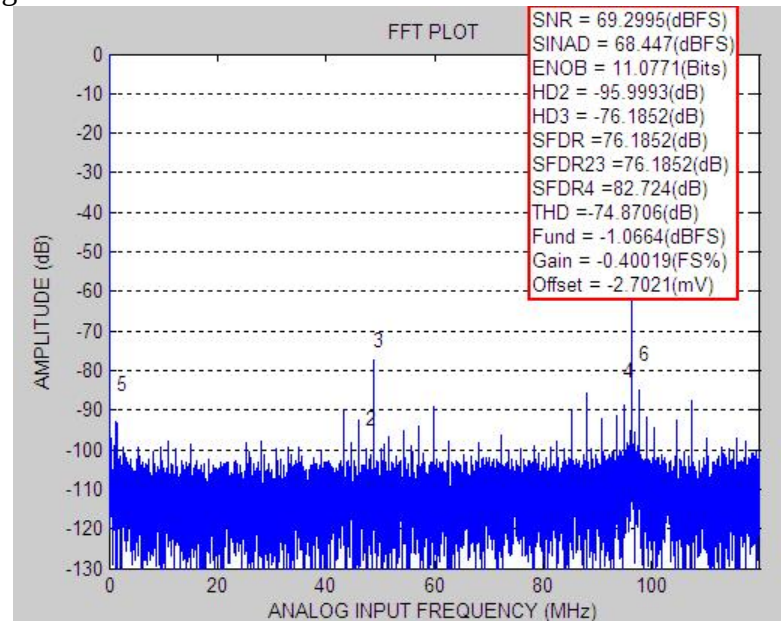

Figure 3. The measured performances of the proposed pipeline ADC.

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