

# The Clock System in Readout Electronics System for the External Target Experiment in CSR of HIRFL

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**Abstract**—A high precision clock system is required in the external target experiment of the Cooling Storage Ring (CSR) project in the Heavy Ion Research Facility in Lanzhou (HIRFL). Considering that the detectors are located in different places of the experimental hall, a high quality clock signal is required to be generated and distributed to multiple measurement modules over long distances. The clock system is based on a master-slave structure: the slave clock module (SCM) receives the clock signal from the master clock module (MCM) through fiber, and then distributes it to the measurement modules within the same PXI crate. Laboratory test results indicate that the period jitter and cycle-to-cycle jitter of this clock system is better than 5 ps and 8.5 ps respectively. We also conducted tests on the TOF (time of flight) readout modules (with the highest time measurement resolution in the readout electronics) combined with this clock system, and a time resolution better than 25 ps is achieved, beyond the requirement.

**Keywords**—cycle to cycle jitter; period jitter; clock skew; LVDS; clock system

## I. INTRODUCTION

The Cooling Storage Ring (CSR) project in the Heavy Ion Research Facility at Lanzhou (HIRFL) consists of a main ring (CSRm), an experiment ring (CSRe), and a radioactive beam line (RIBLL2) to connect the two rings [1, 2]. The external target experiment in CSR is composed of one Start Time Detector, one  $\gamma$  Detector, one Big Dipole, six Multi-Wire Drift Chambers (MWDC), three Time of Flight Walls (TOF Wall), one Neutron Wall, etc [3].

Readout electronics of the main detectors have been designed, and some massive production has been conducted. For example, in the readout electronics of the TOF Wall and Neutron Wall named Time and Charge Measurement Modules (TCMM), both time and charge measurement is required, with a time resolution of 25 ps [4], and 60 measurement modules have been fabricated, corresponding to a total of 960 channels; as for the MWDC, a total of 6400 channels have been implemented (128 channels integrated within each module), and a time resolution of 100 ps is achieved in the digitization module [3]. Since high precision time measurement is required, a high quality clock system is indispensable.

Considering the scale of the readout electronics, the readout modules are integrated in PXI crates, as shown in Fig. 1. Since the detectors are scattered in different places in the experiment

hall, the corresponding readout electronics are also distributed over a large area. Therefore, good quality of the clock signal transmission has to be considered. In the clock system, a master-slave structure is employed. The clock system is implemented as 6U PXI modules, which includes two types: the master clock module (MCM) and the slave clock module (SCM).

As mentioned above, the following difficulties need to be overcome in the design of the clock system:

- 1) Large number of clock signals distributed to different measurement modules ( $\sim 200$  channels);
- 2) Good transmission quality of the clock signal from the MCM to the SCM over a long distance.

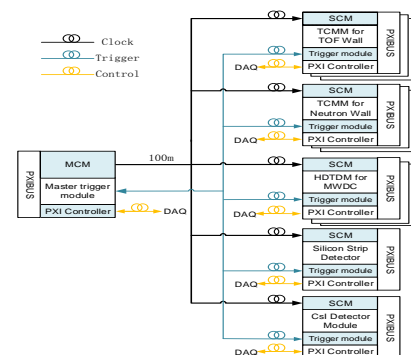


FIGURE 1. ARCHITECTURE OF THE READOUT ELECTRONICS FOR THE EXTERNAL TARGET EXPERIMENT IN CSR OF HIRFL.

## II. IMPLEMENTATION

### A. Architecture of the Clock System

As mentioned above, considering the scale of the readout electronics that is distributed in a large area, this clock system is based on a master-slave structure. In the external target experiment of CSR, the measurement modules for detectors are integrated in 11 PXI crates. Therefore, at least 11 output channels are required in the MCM. Considering the future extension, 20 channels are implemented. To guarantee the clock transmission quality from the MCM to SCM over long distances, optical fibers are used. Due to the size limitation of the PXI 6U module and the package size of the optical transceiver, the MCM is split into two modules --MCM1 and MCM2, each with 10 output channels, as shown in Fig. 2. An

oven crystal oscillator is integrated in MCM1 as the clock source, which is distributed to 10 optical transceivers as the output clocks for the SCMs. MCM1 also outputs another LVDS clock signal, which is transmitted to MCM2 as the clock source to generate other 10 output signals. Except for the clock source, MCM1 and MCM2 share a similar structure.

As for the SCM, each SCM is located within one PXI crate, and it is responsible to provide clock signals for the measurement modules in other slots (13 user slots in each PXI crate). A total of 19 output channels are integrated in each SCM for further extension. Since the transmission path is within 1 meter long between the SCM and the measurement modules; therefore, transmission is based on coaxial cables.

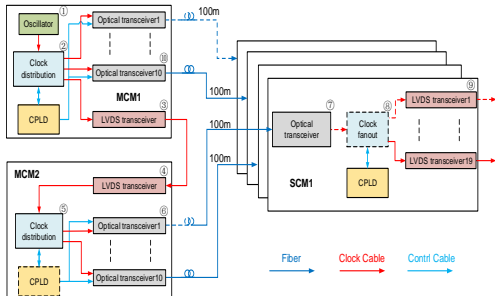


FIGURE II. BLOCK DIAGRAM OF THE CLOCK SYSTEM.

To achieve good jitter performance, the following aspects are considered in circuit design:

1) To enhance the resistance to Electro-Magnetic Interference (EMI), differential processing and transmission is employed for the kernel parts in the Printed Circuit Board (PCB), and the optical fiber is used to reduce the EMI from the environment. Besides, optical transmission also isolates the electronic connection between the central PXI crate (where the MCM is located) and the other PXI crates (where the SCMs are located). Special attention is also paid on signal integrity, such as impedance matching, complete ground layers design, etc.

2) Other attention is paid to device selection.

The accuracy of the clock source determines the quality of output signal. By careful selection, EX-380oven crystal oscillator from the Vectron International company is employed as the clock source, which provides high quality clock for clock system. The cycle-to-cycle jitter of EX-380output is less than 8ps (RMS). The temperature Stability is  $\pm 7.5 \times 10^{-8}$  over  $-20^\circ\text{C}$  to  $+70^\circ\text{C}$  [5].

The buffer and optical transceiver are also the kernel parts of the clock system. We select SY89828L as the buffer (the cycle-to-cycle jitter less than 1ps) [6], and it can fan out 20 LVDS outputs. FTLF8524P3NL is employed as the optical transceiver. The outputs of the SY89828L are differential signals, which are AC coupled at the input of the optical transceiver, and terminated by the internal  $100\ \Omega$  differential resistor inside FTLF8524P3NL [7].

### B. Hardware Control Logic and PXI Interface

To configure the clock system on line, a CPLD is employed to integrate the PCI interface to communicate with

the host computer located in Slot 0 of the PXI crate, This CPLD receives the commands from the host computer through the PXI bus, and decodes them to different configuration data, including the clock source selection on the MCM, enabling of different clock output channels, as shown in Fig. 3. The PCI IP Core pci\_mt32 (from the Altera Corporation) [8] is employed to bridge between the PCI Bus and Target Control Logic that translates the message from the PXI bus to configuration data.

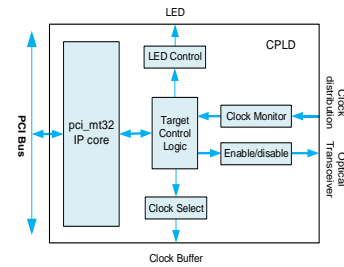


FIGURE III. BLOCK DIAGRAM OF THE LOGIC DESIGN IN THE CPLD.

This CPLD also monitors the clock status in the SCM. The clock distributor in the SCM distributes 20 output signals, among which 19 signals are used as the outputs of the SCM, and the other one is imported to the CPLD. As shown in Fig. 4, this 40 MHz clock is converted in the CPLD to a 400 kHz low frequency signal, which is used as the “Start” and “Stop” signal of a 33 MHz counter. By analyzing the output of the counter, the status of the clock signal can be monitored in real time. When an error is detected, the CPLD will request an interrupt through the PXI bus to the host computer.

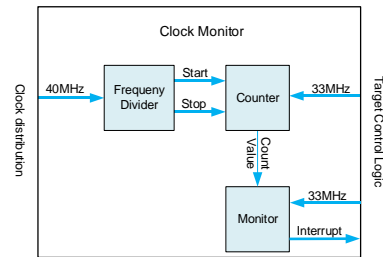


FIGURE IV. BLOCK DIAGRAM OF THE CLOCK MONITOR BLOCK.

We have designed 2 MCMs and 6 SCMs; the photographs of the MCM and SCM are shown in Fig. 5.

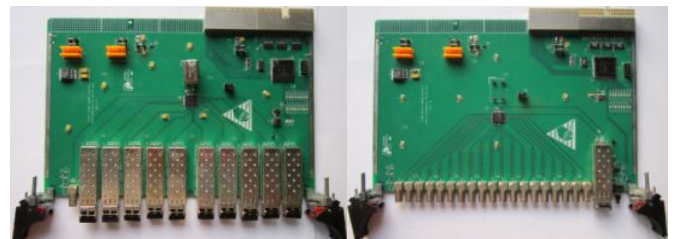


FIGURE V. (A) PHOTOGRAPH OF MCM; (B) PHOTOGRAPH OF SCM.

### C. Test Software

In each PXI crate, there is one host computer which is responsible for reading out the data from the modules within it, as well as configuring these modules. We designed test

software running on this host computer based on Visual C++ and WIND river. A graphical user interface (GUI) is designed for user input, as well as display of the system status, as shown in Fig.6. The commands can be sent to the clock modules by clicking on different buttons.

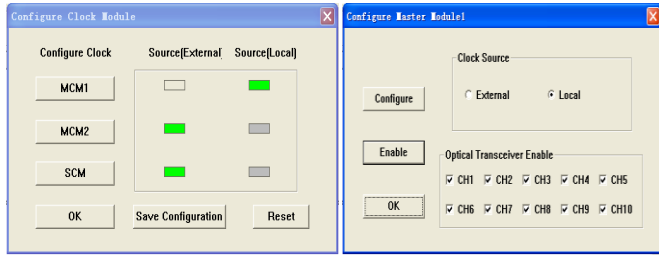


FIGURE VI. (A) THE STATUS INTERFACE OF CLOCK SYSTEM; (B) THE CONFIGURATION INTERFACE OF MCM.

### III. TEST RESULTS

To evaluate the performance of this clock system, we conducted a series of tests in the laboratory.

#### A. Laboratory Test Configuration



FIGURE VII. SYSTEM UNDER TEST.

In the laboratory tests, we focused on two parameters: one is the jitter of the final clock signal, and the other is the skew among different output channels. Fig. 7 shows the system under test. A high speed oscilloscope Wave Runner 640Zi (40 GS/s with an analog bandwidth of 4 GHz) is used to capture the waveforms of the output clock signals and analyze the performance with the software WR6Zi-JITKIT on it. We used this software to conduct the statistical analysis, plot histograms, and finally obtain the cycle-to-cycle jitter, as well as the period jitter.

#### B. Result of Clock Jitter

In the tests, we first captured the waveforms of the final output clock signal. Shown in Fig. 8 is atypical persistence diagram of the clock signal waveform, which indicates that the clock signal concurs well with the LVDS standard with no obvious distortion and dispersion among these accumulated waveforms. To obtain the jitter value, we performed statistical analysis with the oscilloscope. A typical histogram of the clock period is shown in Fig. 9, in which the mean value of the clock period is 25.0026 ns (conforms well with the expected 40 MHz clock frequency) and the standard deviation (i.e. period jitter) is 4.01ps. The period jitter can also be obtained through the software WR6Zi-JITKIT.

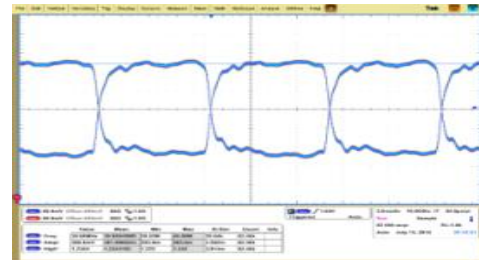


FIGURE VIII. PERSISTENCE DIAGRAM OF THE CLOCK SIGNAL.

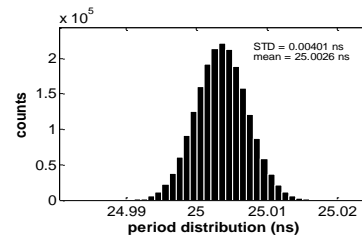


FIGURE IX. TIME MEASUREMENT TEST RESULT OF THE CLOCK PERIOD.

With different connections between the MCM output channels and SCMs, the performance of the SCMs output clock would be different. Shown in Fig.10 is the jitter performance of all the 144 output channels, with the 6 SCMs connected to the MCM output channel that has worst performance. Fig. 10(a) and (b) correspond to the cycle-to-cycle jitter and the period jitter results, respectively. The cycle-to-cycle jitter is better than 8.5 ps and the period jitter is better than 5 ps.

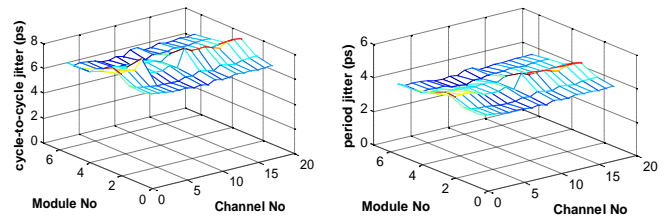


FIGURE X. (A) CYCLE TO CYCLE JITTER OF 114 CHANNELS; (B) PERIOD JITTER OF 114 CHANNELS.

We have also conducted long-term stability tests of 12 hours. The test results were recorded every half an hour. A typical test result is shown in Fig. 11, and the cycle-to-cycle jitter test results are quite stable.

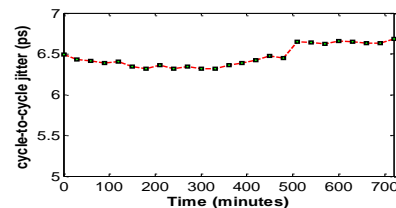


FIGURE XI. RESULT OF LONG TERM STABILITY TEST.

As shown in Table 1, we also compared the performance of this clock system with those in some well-known physics experiments [9, 10, 11, 12]. The jitter performance (cycle-to-cycle jitter < 8.5 ps and period jitter < 5 ps in worst case) of

this system is good enough.

TABLE I. JITTER PERFORMANCE OF THE CLOCK SYSTEMS IN SOME WELL-KNOWN PHYSICSEXPERIMENTS.

physicalexperiment	BESIII	BELLE	Alice	Daya Bay
Jitter (ps)	11	20	10	500

### C. Skew Test Results

We conducted tests to estimate the clock skew among different output channels. As shown in Fig.12, the output of the MCM is transmitted to the SCM through 100 meter fiber, and we tested the skew between the outputs of the SCM. In the tests, we swapped the connection between the test cables and the output connectors of SCM, in order to eliminate the additional skew introduced by the test cables and the measurement channels of the oscilloscope.

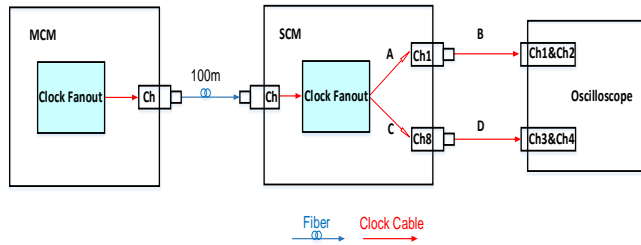


FIGURE XII. BLOCK DIAGRAM OF SKEW MEASUREMENT.

The skew test results between Channel 8 and the other 18 output channels of the SCM are shown in Fig. 13, in which the maximum skew value is around 40 ps.

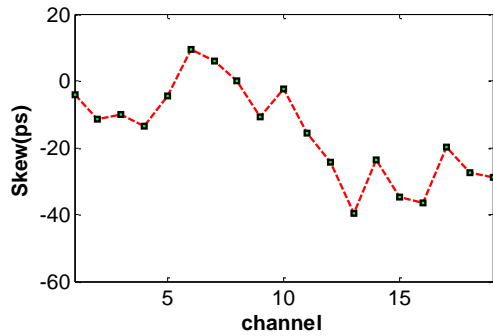


FIGURE XIII. SKEW TEST RESULTS.

Shown in Fig. 13 are the skew test results in the laboratory. Of course, in actual experiment setup, we will conduct tests to calibrate the delay difference among all the time measurement channels in the readout electronics, including the delay introduced by the cable between the detector and the electronics, the circuit delay of the electronics channels, as well as the clock delay of each measurement module.

### D. Initial Joint Test Result between TCMM and Clock System

Considering that a 25 ps time resolution is required on the TCMM within the readout electronics, we conducted tests on the TCMM with the clock system to further evaluate its performance. Fig. 14 shows the test results of the TCMM; a time resolution better than 25 ps and a charge resolution better than 8% are achieved in the input amplitude range from 50 mV to 2.5 V, which is better than the requirement.

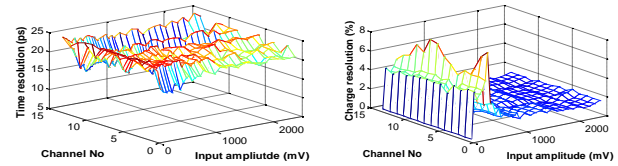


FIGURE XIV. (A) TIME RESOLUTION OF THE 16 CHANNELS; (B) CHARGE RESOLUTION.

## IV. CONCLUSIONS

A clock system is designed for the readout electronics of the external target experiment of the CSR in HIRFL. A Master-Slave structure is employed, with the clock transmission based on fibers. We have fabricated 2 MCMs and 6 SCM, and test results indicate that the period jitter and cycle-to-cycle jitter of this clock system is better than 5 ps and 8.5 ps, respectively. And the combination tests between the TCMM and the clock system were also conducted, and a 25 ps time resolution is achieved, which meets the application requirement.

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## REFERENCES

- [1] Zheng C, Xiao Z, Xu H, et al. Hadron Physics Programs at HIRFL-CSRm: Plan and Status, High Energy Physics and Nuclear Physics, 2007, 31(12): 1177-1180.
- [2] Xia J, Zhan W, Wei B, et al. The Heavy Ion Cooler-Storage-Ring Project (HIRFLCSR) at Lanzhou, Nuclear Instruments and Methods in Physics Research A, 2002, 488: 11-25.
- [3] ZHAO Lei, KANG Longfei, ZHOU Jiawen, et al. A 16-Channel High-Resolution Time and Charge Measurement Module for the External Target Experiment in the CSR of HIRFL, Nuclear Science and Techniques, 2014, 010401:1-6.
- [4] Zhou J. Ph.D. Thesis, University of Science and Technology of China, 2012.
- [5] VECTRON Corporation. EX-380 series 4 pin DIP & SMD evacuated miniature crystal oscillator product data sheet, <http://www.vectron.com/products/ocxo/2001>.
- [6] 3.3V 1GHz dual 1:10 precision lvds fanout buffer/translator with 2:1 input mux. [http://www.mierel.com/\\_PDF/HBW/sy898281.pdf](http://www.mierel.com/_PDF/HBW/sy898281.pdf).
- [7] 3.7 Gb/s RoHS Compliant Short-Wavelength SFP Transceiver FTLF8524P3BNL. [http://www.finisar.com/sites/default/files/pdf/FTLF8524P3BNL\\_3.7Gbs\\_Short-Wavelength\\_SFP\\_Transceiver\\_Spec\\_RevB.pdf](http://www.finisar.com/sites/default/files/pdf/FTLF8524P3BNL_3.7Gbs_Short-Wavelength_SFP_Transceiver_Spec_RevB.pdf).
- [8] PCI Compiler User Guide, 2005. [http://www.altera.com/literature/ug/ug\\_pci.pdf](http://www.altera.com/literature/ug/ug_pci.pdf).
- [9] Hao Li, Shubin Liu, Changqing Feng, et al. TOF Clock System for BES III, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 2, APRIL 2010.
- [10] A. Abashian, K. Gotow, N. Morgan, et al. The Belle detector, Nuclear Instruments and Methods in Physics Research A 479 (2002) 117-232.
- [11] L. Colombini, M. Lippi, A. Mati, et al. Compact data acquisition and power supply system designed for hostile environment condition concerning radiation and magnetic field, <https://cds.cern.ch/record/921196/files/p346.pdf>.
- [12] Poster - Daya Bay Reactor Neutrino Experiment, [http://dayabay.ihep.ac.cn/pubtalk/TIPP09\\_linyc\\_poster1\\_high\\_resolution.pdf](http://dayabay.ihep.ac.cn/pubtalk/TIPP09_linyc_poster1_high_resolution.pdf).