Design of General Vehicle Bus Testing System

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Abstract. Aiming to the problems that the current vehicle bus test technology just realizes the test of DLL and the test equipment is not universal this paper brings forward a universal test method to the vehicle bus based on Data Frame Collecting technology and Software Decoding technology designs the physical layer test system to the universal vehicle bus. It's convenient to locate the fault and provide solid judgments for maintenance.

Introduction

Vehicles, especially armored vehicles, are equipped with more and more electronic equipment's which are becoming more and more complex. It brings new problems to equipment maintenance. One is that the difficulty of maintenance and support of communication system equipment's has increased; the other is that when these the on-board equipment's are used in network, it is difficult to locate fault points of failure, lack of monitoring means, and cannot be ruled out faults. The main buses used on military vehicles are 1553b bus, CAN bus, MIC bus, etc. the running status and working performance of Vehicle bus directly affects performance and security of on-board equipment's. At present it lacks of full and accurate method of test for the serial bus. There are some difficulties of bus troubleshooting and positioning, and can't provide detailed basis for the maintenance support.

The deficiency existing in the current bus test method

It lacks of general bus test equipment. At present a variety of vehicles are using all kinds of bus types, but it lacks of integrated general bus test equipment to test functions of the multi-types bus. Each bus has different protocol, chip and interface, which leads to difficulties of hardware compatibility. When testing the bus we need to choose corresponding bus interface adapter, which leads that the volume of the measuring equipment of integrated electronic system is too big. It cannot meet the demand in situ testing and is difficult to realize a wide range of application and dissemination.

The data frame getting from the bus protocol chip is not comprehensive. Bus interface module can directly receive bus transmission waveform and interpret into data frame. It will also filter the error frame and the data frame which is unable to interpret correctly. These error frame are the key data on analysis for the cause of the system problem .When the system fails, it will not be able to accurately determine whether sender, recipient, line matching device or the transmission line itself due to lack of these error frame data.

We can't measure the electrical properties of the bus using the bus interface module. Bus interface module only implements the test of the data link layer. You can't measure electrical performance on serial bus, and can't find fault in the physical layer.

Overall design of the system

Design of hardware. Gm vehicle serial bus test system is mainly composed by the high-speed data acquisition equipment, large-capacity and high-speed storage devices, the core processor, display systems and related equipment. The system is mainly based on embedded ARM platform and high-

speed data acquisition card and processing board. It innovatively uses the technology in balance of storage of high-speed data, secondary data cache technology, time calibration technology after receiving a data frame, etc., with a high-speed data acquisition and storage of bus waveform for a long time, the data link layer data analysis, and other functions. The system structure is shown in figure 1.

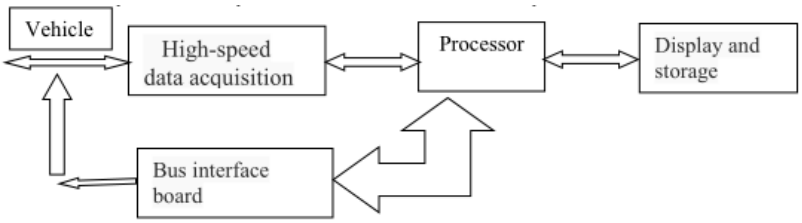

Fig.1. the system structure

The High-speed data acquisition board. FPGA high-speed data acquisition card is adopted in this design, as shown in figure 2, the card has 2 roads of 20 MHz high-speed acquisition channel .In each road, front-end data acquisition part and AD converter part are used independently. Two-road channels share 512M first-in, first-out (FIFO) storage. Acquisition card communicate with the host through PCI interface, supporting 132 MBytes/s high-speed bandwidth and 30 MS/s and high speed continuous acquisition. It can transfer data to the host at top 50 MBytes/s (PCI maximum transmission rate) by the way of PCI DMA, which is able to meet the needs of bus test system designed in this paper.

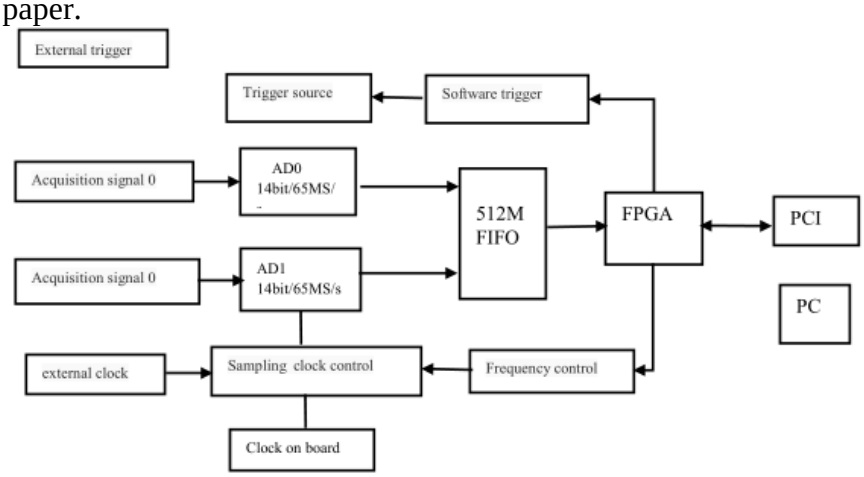

Fig.2 The principle of high-speed data acquisition card

In order to meet the requirements of high-speed data acquisition, acquisition card use the cache memory technology. As shown in figure 3, the first cache uses SODIMM SDRAM, and the second cache uses BUF2 FIFO. SODIMM SDRAM has optional size (128 M / 256 M / 512 M) and fixed size of BUF2 is 8404992 Bytes (8 MB + 16 kB). The acquisition software can read the size of FIFO in BUF2, and if two caches are full, buffer overrun, then there will be a loss of data.

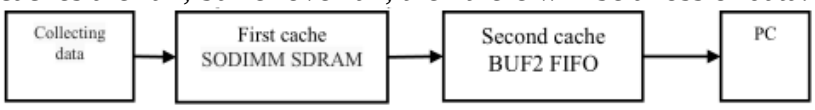

Fig.3 The design of cache memory

The core processing module. This design chose Samsung's latest S3C6410 microprocessor based on ARM1176JZF-S kernel as the main controller. S3C6410 microprocessor has rich integrated function, leaves out the design of the peripheral hardware circuit such as SPI, USB and ADC, saving the cost of the system, and improves the reliability of the system. It is very suitable as a main control unit of portable test equipment.

The large capacity storage module. Because some bus communication rate is higher, collection for a short period of time will produce large amounts of data. From the aspects of storage capacity, read and write speed and cost, this design considers using multiple of hard disk to form RAID disk array for long-time storage carrier of the high-speed data acquisition system. System with data requests can be parallel executed through multiple disk. Each disk performs its own portion of the request, to

provide higher literacy rate and more storage space than single disk. The disk group can not only satisfy the requirement of the physical test system of high-speed data acquisition for a long time, can also meet the requirements of the system of large capacity storage.

In this paper, the general design of vehicle serial bus test system adopts the RAIDO physical disk array control technology to hook up the 2 piece of 500 gb SATA hard disk, measured with hard disk read and write speed test software: in the 256 kBytes block transmission mode, the disk write speed reached more than 200 MB/s, so it can completely satisfy the system application requirements in terms of the disk write speed.

Design of software. The structure of software of the General vehicle serial bus test system includes the test application and the driver. Application has the function of the main test management module, data collection and storage module, data processing module, data analysis diagnosis display module; the driver is mainly A/D acquisition card driver.

As shown in figure 4, the system is divided into four modules: test management (SAD Manager), data acquisition and storage (SAD Capturer), data analysis (SAD Analyzer), and data display (SAD Output).

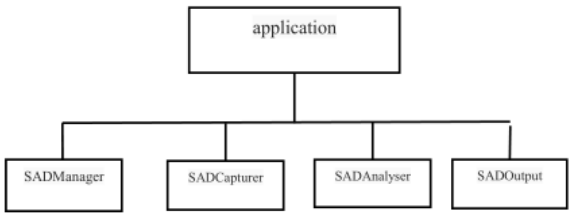

Fig.4 The system software

SAD Manager. Test management module is mainly used to receive the user's Settings information, launch the test task, realize the testing task management, basic parameter Settings, function setting, data query and user management, etc. The content of test management is the current name and time, bus type, test record; Parameter setting is to set global parameters for the specific testing tasks, including the communication rate, parity, start bit, the number of data bits, frame format and the parameters of the control command, etc.; Functional configuration according to the different to set up the testing tasks allocation function; History data query is to provide The query and playback of the test data; User management is used for users increase, delete, modify, and user permissions Settings, and so on.

SAD Capturer. Data collection and storage module realizes real-time data collection and record according to the bus control command, and storage group package in accordance with the relevant communication interface file, as a basis for decoding, the basis of analysis, locate fault, and according to the configuration parameter to determine whether to display real-time data signal waveform, or decoding the data, etc.

SAD Analyzer. After data acquisition is done, the tester will analyze the collected data, realizing fault diagnosis, orientation and process quickly, mainly according to the different test demand of equipment. The module has the following functions: (1) to complete the physical data waveform analysis of all bus data; (2) to automatically calculate the bus baud rate; (3) to identify all sampling data frames or message types, according to the baud rate and the sampling rate; (4) to calculate the interval time between adjacent frame or message word; (5) to complete the query of specific characters.

SAD Output. Display output module is mainly used to implement the data waveform display, records of the process and results of diagnosis, the output and printing, etc. Graphics include signal level figure, sampling waveform figure, decoding data graph.

Experimental verification

This test system was designed for several common vehicle serial bus, CAN bus and 1553 B bus and the MIC bus for comprehensive performance test, including the physical performance test and performance test of data link layer, and through the analysis of the results to judge the transmission

performance of current vehicle bus network . In this test we take CAN bus as an example for experiment.

Physical properties testing of CAN bus network. Connect a single test nodes to CAN bus node transceiver. Connect the probe of dual channel respectively to CAN_H and CAN_L of the test nodes. CAN bus network transceiver sends a frame to the CAN bus network data frame per 50 ms. Set the general bus test system to collect and store data collected. From figure 5, you can see that the transmission signal level collected from the CAN bus is more smooth, with no burr.

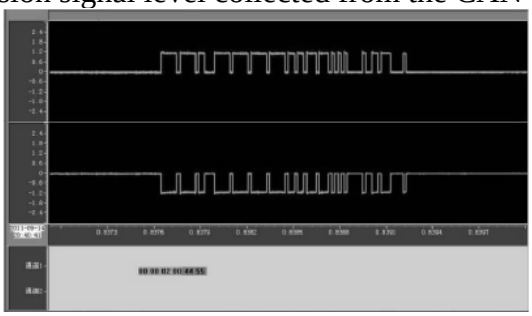

Fig.5 Bus signal waveform

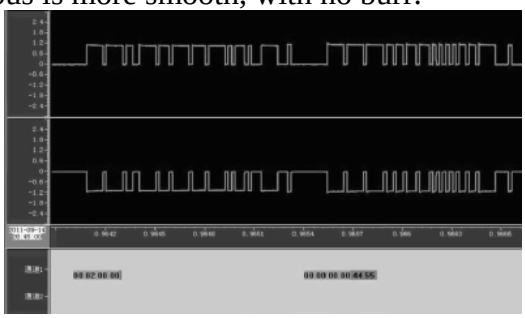

Fig.6 the results of the analysis

Baud rate identification test of CAN bus network. The general bus test system is connected to the CAN bus network. The data is collected and stored in the hard disk. The baud rate is calculated by the system software. The resolution of bus network transmission rate is 50k.

Data acquisition analysis test of CAN bus network. Connect the general bus test system to the CAN bus network, CAN bus transceiver 1 send a standard data frames per 50 ms and CAN bus transceiver 2 send a extending remote frame per 50 ms and the length of standard data frame is 2 bytes, the value is 44 55. General decoding software analyze the data bus transmission signal based on the analysis of collected data, as shown in figure 6. There are two kinds of signals on bus. One is a remote frame, the other is a data frame, and its value is 44 55. This shows that in this paper, the design of the CAN bus data acquisition module can fully analyze the CAN message frame, and complete the tracking and acquisition of can bus data.

Summary

With several common vehicle serial bus, CAN bus and 1553 B bus and the MIC bus, are more and more widely used on the military vehicle electronic system, testing methods are more and more, and becoming more and better. In this paper, the general vehicle serial bus testing technology, uses the high-speed acquisition technology, the cache memory technology and mass storage technology to design the general vehicle serial bus test system. It can be used on the current vehicle bus system for comprehensive test, to facilitate bus fault locating, and provide detailed basis for the maintenance test.

References

[1]Wang Liming, Shao Ying, Wang Mingzhe. Research of improving the dynamic scheduling algorithm in the CAN bus control networks. Journal of Systems Engineering and Electronics, 2008, 19(6): 1250-1257

[2]Zeng C H, Pan M, Wang S Y. CAN bus communication system based on SOC technology [C]. Intelligent Computing and Integrated Systems (ICISS), 2010 International Conference on. IEEE, 2010: 322-325.

[3]Li Ran, Wu Junfeng, Wang Haiying. Design method of CAN BUS network communication structure for electric vehicle [J] .Strategic Technology (IFOST), 2010(10):326-329.

[4]LUO Y, CAI S. Design and Implementation of Interface Based on 1553B Bus [J]. Modern Electronics Technique, 2006, 2: 022.

[5]Duwei Y, Jianzhong Z, Lei Z. Implementation of Communication Board Based on 1553B Bus [C]. Electronic Measurement and Instruments, 2007. ICEMI'07. 8th International Conference on. IEEE, 2007: 1-837-1-840.