Effects of Soft Information Quantization Precision on LDPC Performance for NAND Flash Application

Changlai SONG[1, a], Haozhi MA[1,b] and Liyang PAN[2,c]

[1]Institute of Microelectronics, Tsinghua University, Beijing, China

[2]Graduate School at Shenzhen, Tsinghua University, Shenzhen 518055, China

[a]songchanglai1990@gmail.com, [b]mhz10@mails.tsinghua.edu.cn, [c]panly@tsinghua.edu.cn

Keywords: LDPC; NAND Flash; simulation; AWGN.

Abstract. (17664, 16512) LDPC code is simulated under AWGN channel. The simulation is led on FPGA platform, with Layered Normalized BP-Based decoding algorithm. The shifting of measurement point is under consideration, where the soft information for decoding is inaccurate. LDPC performance under different situations are compared, and performance decreased rapidly with measurement point shifted. The related research results may provide a key basis for LDPC application in NAND Flash controller.

Introduction

Due to the ever-decreasing semiconductor technology size, NAND Flash appears to have increasingly higher raw bit error rate(RBER), which needs to compensate for the low error rate through the embedded error correction circuit (ECC) in the NFC controller(generally around 10^{-15} to 10^{-12} magnitude) [1]. Because of the mature coding theory and the simple circuit, the existing NFC circuit is mainly based on BCH cyclic codes of hard decision circuit to help the error correcting digits reach 72 bits (corresponding RBER can reach 10^{-6} to 10^{-5} magnitude) [1]. However, with the NAND Flash unit processes shriveling to 1X nm node and the application of MLC/TLC technology, NAND Flash unit raw bit error rate soars to 10^{-3} magnitude, even up to 5×10^{-3} [2], the existing BCH code error correction capacity can not meet the requirements of application.

As low density parity check code (LDPC) of soft decision can make full use of the unit threshold distribution to acquire higher error correcting bits at the same redundancy cost, it has received extensive attention in recent years [3]. The ECC system applied to the area of memory is more concerned with rate (the proportion of information bits representing the entire code word) than in the field of communication. Because the utilization efficiency rate directly affects the cost of storage unit, LDPC code rate directly determines the number of bits of redundant and the hardware cost of system, and its structure will affect the complexity and performance of the ECC circuit. Therefore, studies have mainly focuses on the different structure of LDPC code, with the highest rate reaching more than 93% [3].

At the same time, studies show that the error correction capability of LDPC code is related with the quantification precision and accuracy of soft information, in the NFC application. It mainly obtains quantitative information of V_t distribution via Read Retry technology, but Read Retry technology need to start multiple NAND Flash read operation, which has a great impact on reading performance of NFC system [4]. More study shows that NAND Flash appears the degradation effect of Endurance and Retention characteristics after multiple erase cycle operation and long-term preservation [4], which leads to V_t distribution shifted and measurement deviation of soft information , and then leads to the degeneration of the error correction capability of LDPC codes. Therefore, it is very necessary to study the fluctuation characteristics of soft information of V_t distribution and its effect on the performance of LDPC code error correction for NAND Flash after multiple erase cycle operation and long-term storage.

Based on the RBER testing of the real NAND Flash devices, this study quantifies for the influence of V_t drift on the soft information, and simulates LDPC error correction performance after the drift. The related research results may provide a key basis for LDPC application in NAND Flash controller.

Test and Method

The simulation uses FPGA as the main experimental platform and DE4 development board of Terasic company as the main hardware. The experiment uses the Qsys function to build a system on a chip, and then uses the Nios II system to write soft code to do Codec simulation performance by controlling system on a chip. Simulation process shown as in Fig. 1.

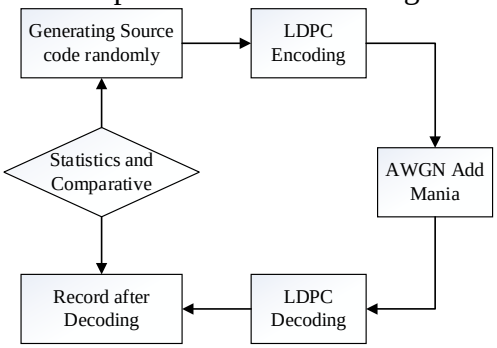

Fig. 1 the Simulation Process

In order to more concisely and intuitively reflect the degradation of LDPC performance when the measurement point shifts, simulation adopts AWGN channel as the original model. By fixing the mean and adjusting the variance of the normal distribution to achieve the purpose of controlling the raw bit error rate.

The original code is generated randomly which can ensure uniform coverage of the sample. Decoding circuit adopts the Layered Normalized BP-Based algorithm [7] to design so that it can save more circuit resources and be more suitable for hardware circuit as well as more in line with the real scenarios. Principle structure of the decoding circuit shown as in Fig. 2.

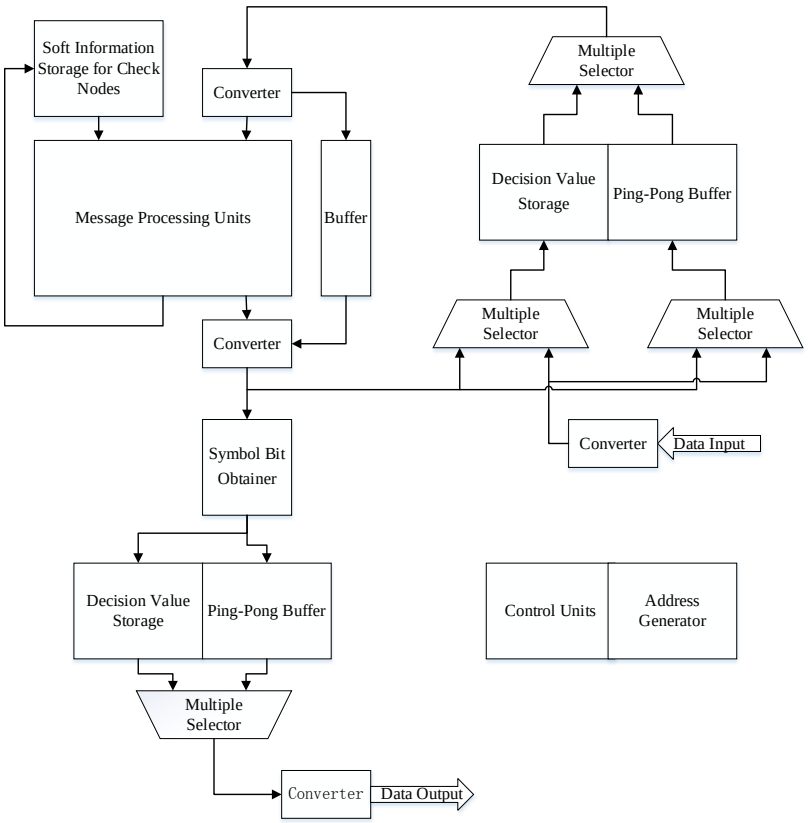

Fig. 2 Principle Structure of the Decoding Circuit

Decoder soft information uses 6Bit quantification accuracy and the maximum number of iterations is 50 times. One of the Bits in 6Bit soft information is the sign bit, and the other 5 Bits are data bits. According to the LDPC decoding theory, the higher quantification precision and the more iterations will have better performance. Taking into account the actual circuit, obtaining highly accurate quantitative information needs multiple Read Retry, and too many iterations will greatly increase the decoding delay. Therefore, in this simulation, the quantification precision is 6Bit and the maximum number of iterations is 50 times

In order to be closer to practical application of NAND Flash, LDPC codes used in the simulation adopts specific code length and has a high bit rate. The specific parameters are (17664, 16512), with code rate as high as 93.5% [8]. This code is a system code and has a quasi-cyclic structure, easy for circuit implementation. The code is constructed via Fourier transforms and row and column permutations, which has an error floor lower than 10^{-15} [8].

In addition to the circuit, another important issue of the simulation to be solved is the definition of soft information, especially how to define the soft information measurement point shifted.

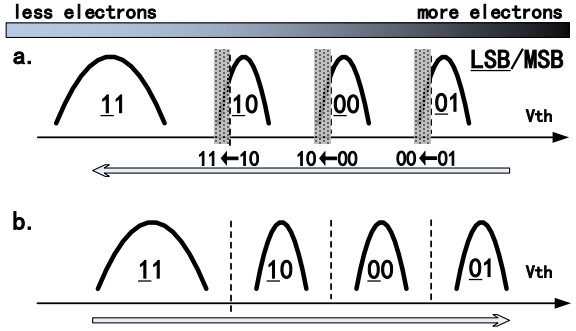

Fig. 3 Principle Structure of the Decoding Circuit

In the practical application of NAND Flash, the related research shows that NAND Flash appears the degradation effect of Endurance and Retention characteristics after multiple erase cycle operation and long-term preservation, leading to V_t distribution of drift. As shown in Fig. 3.

In experiments with real NAND Flash devices, it is found that numbers of different error pattern vary a lot, sometimes in different situation of retention time and P/E cycles one error pattern can have two times the frequency than another. As shown in Fig. 4 below.

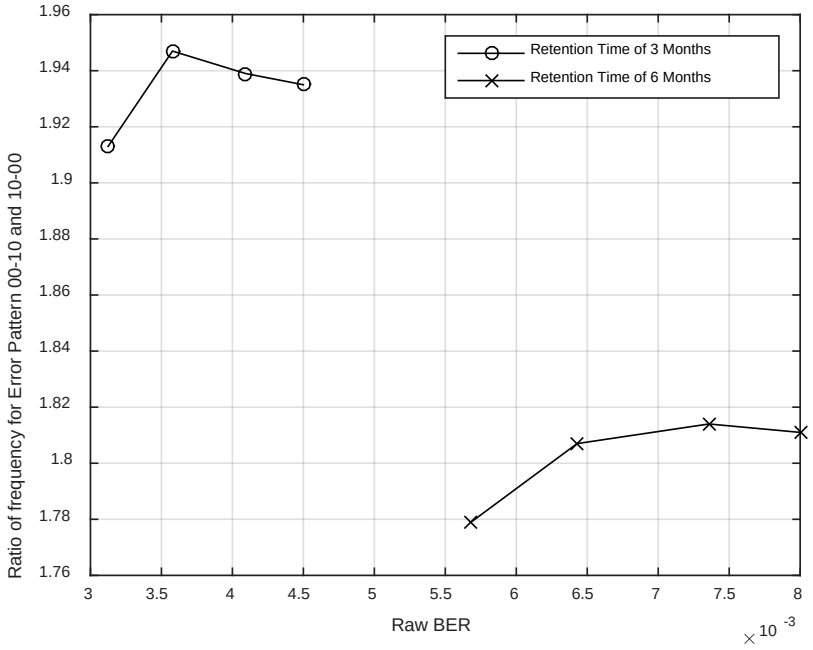

Fig. 4 Error Pattern Ratios

The physical meaning of the ratios is the ratio of the area of the voltage distribution corresponding to the two states, on one side of measurement point.

In order to more intuitively reflect V_t distribution shifted, the simulation consider the most basic the double normal distribution. And in situations when there are more distributions, e.g. MLC or TLC, principle will be similar because comparison voltage is relatively independent, and it could be divided into several double normal distributions.

When there is no V_t offset, the comparing measured voltage is just at the symmetry point of two normal distributions, as shown in Fig. 5. Since simulation adopts 6Bit accuracy, when doing the specific simulation operation, 31 intervals would be taken from both the left and right sides of the measurement points to be quantified directly, and then transformed into 6Bit binary number and brought into the decoder for decoding operation. All of the positions over 31 would be recorded as 31 (the reverse of the part plus minus directly), the relative width of quantification interval would be specified the interval indicated by the normal distribution curve peaks. In this simulation, the peak position would be specified as the forty-second interval from the measurement point. Value of soft information represents relative value of $V_t/V_{tm}\times c$, where V_{tm} represents the most probable value of V_t in a particular state, which varies by states and devices, and c is a the constant chosen for LDPC decoding and fitted as 42 in this test.

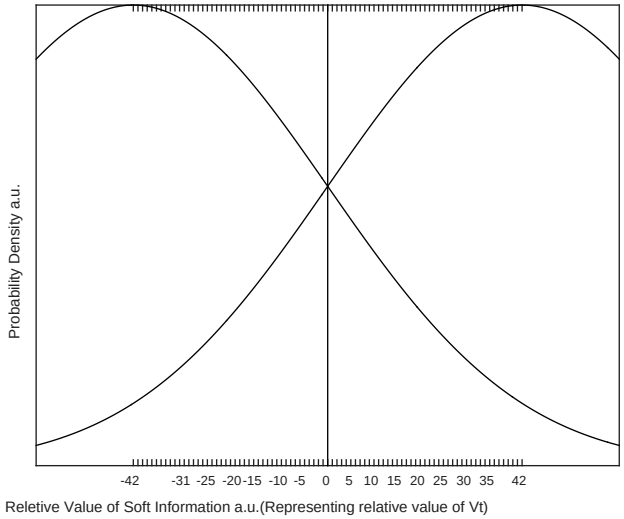

Fig. 5 Soft Information Definition

In the ideal situation, the V_t shift is 0, that is, the measurement point is exactly in the middle of the two normal distributions, as shown in Fig. 5. But when there is V_t shift, if the same read voltage is used to obtain the soft information, the soft information obtained will be not accurate. The V_t distribution shift can be equivalent to the measurement point of soft information shifts. As shown in Fig. 6, measurement point shifted causes soft information is actually not accurate.

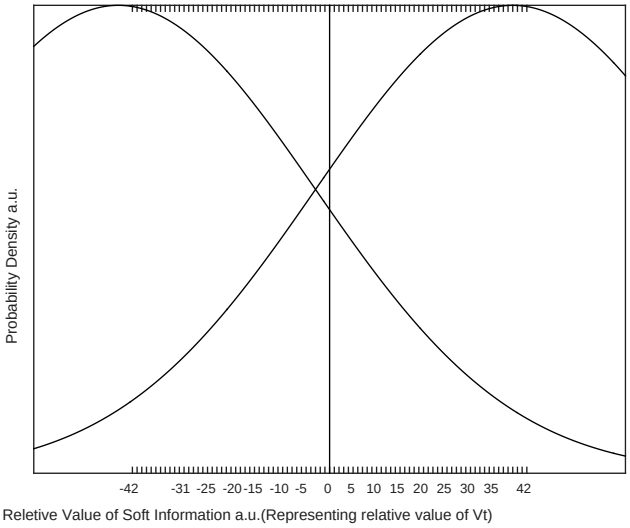

Fig. 6 Measurement Point Offset Causing the Inaccurate Result of Soft Information

Results and Analysis

The experiment simulates the LDPC performance curve with the raw bit error rate from 7.1×10^{-3} to 7.9×10^{-3}. The non-shift curve is shown in Fig. 7. It can be seen in the interval from 7.1×10^{-3} to 7.9×10^{-3}, the attenuation of performance is quite obvious. Due to the obvious performance change of this interval, it is selected as performance simulation interval when considering the shift.

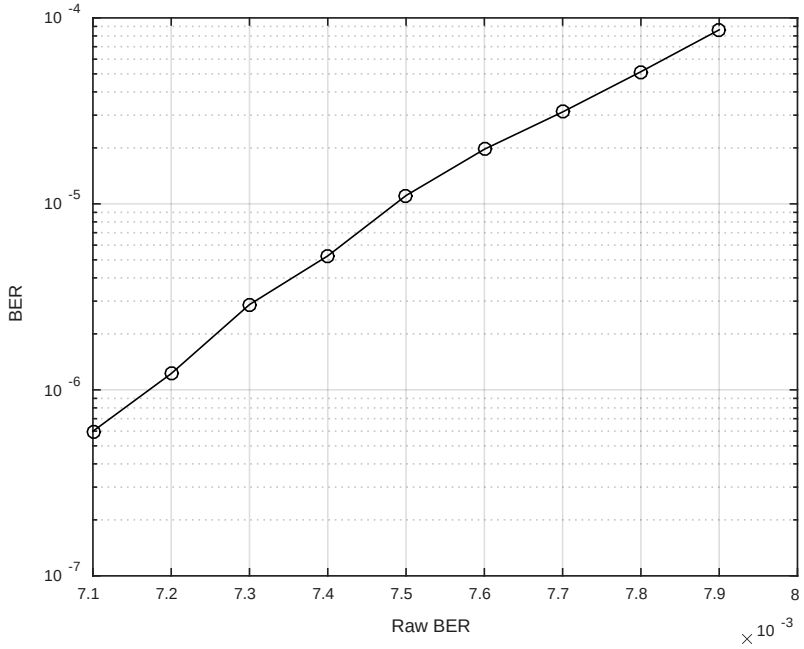

Fig. 7 Performance Curve without Considering the Shift

When the measurement point shifts, it is equivalent to the soft information shifted to left or right unitedly at the time of judgment. The offset value in Fig. 6 represents offset incremental value information of the 6Bit accuracy of quantitative information, for example, if the accurate soft information without considering the shift is a, then when the offset is b, the equivalent soft information is a+b. Matching with the experiment results in Fig. 4, the maximum shift is 3. Fig. 8 simulates the LDPC performance curve with the soft information shift. It can be seen that the measurement point offset not only have great influence to the error correction performance, but also the growth of the offset will accelerate the attenuation.

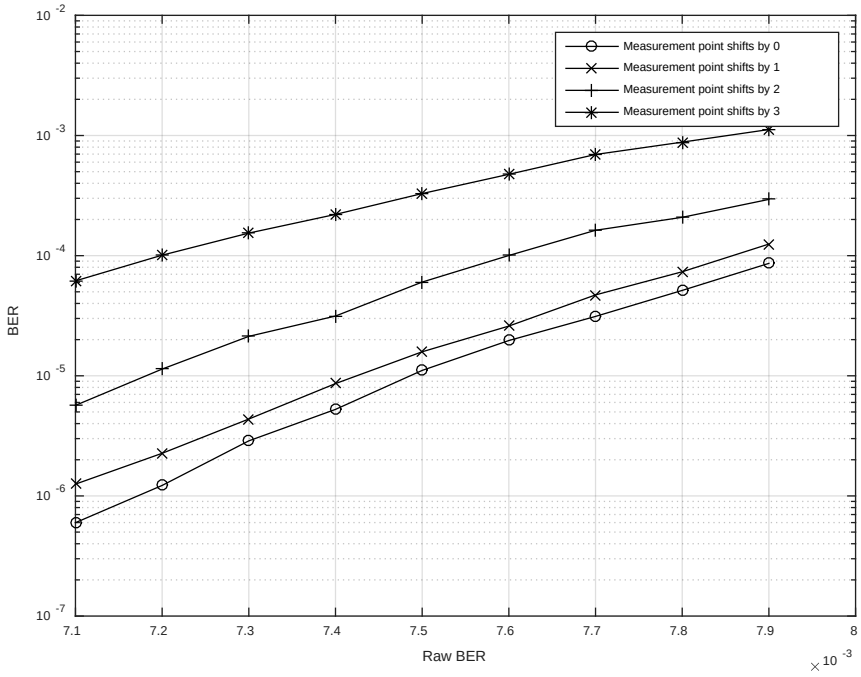

Fig. 8 Performance Curve Considering the Shift

Summary

The results of simulation experiments show that, the measurement offset will cause a great impact on the LDPC error correction performance, and the growth of the offset will accelerate the attenuation. Therefore, in the practical applications, it needs to introduce a specific inspection mechanism, when LDPC error correction performance decreases obviously, it can adjust the comparing voltage timely to improve the gathering mechanisms of soft information, striving to eliminate the influence of V_t distribution shifted for soft information.

Acknowledgments

The work is supported by Chinese National Key Basic Research Program (No.2011CBA00602) and National Key Scientific and Technological Project (No. 2013ZX01032001-001).

References

[1] Xu, X.; Huang, H.H., Exploring Data-Level Error Tolerance in High-Performance Solid-State Drives, *IEEE Trans. on Reliability*, Page(s): 1-16,2014

[2] Korkotsides S.; Bikas G.; et al., BER analysis of MLC NAND Flash memories based on an asymmetric PAM model, *ISCCSP*, Page(s): 558- 561, 2014.

[3] Jonghong Kim; Dong-hwan Lee; et al., Performance of rate 0.96 (68254, 65536) EG-LDPC code for NAND Flash memory error correction, *2012 IEEE Int. Con. on Communications*, Page(s): 7029-7033, 2012.

[4] Cai Yu; Haratsch E. F; et al.; Threshold voltage distribution in MLC NAND flash memory: Characterization, analysis and modeling, *Design, Automation & Test in Europe Conference & Exhibition*, Page(s): 1285-1290, 2013.

[5] R.G.Gallager, Low-Density Parity-Check Codes, *IRE Transactions on Information Theory*, vol.IT-8: 21-28, 1962.

[6] Guiqiang Dong, Ningde Xie and Tong Zhang, On the Use of Soft-Decision Error-Correction Codes in NAND Flash Memory, *IEEE Trans. on Circuits and Systems I: Regular Papers*, 58(2): 429-439, 2011.

[7] Jonghong Kim, Junhee Cho and Wonyong Sung, A High-Speed Layered Min-Sum LDPC Decoder for Error Correction of NAND Flash Memories, *2011 IEEE 54th Int. Midwest Symp. on Circuits and Systems*, pages: 1-10, 2011.

[8] Qiuju Diao; Qin Huang; Shu Lin; Abdel-Ghaffar, K., A transform approach for analyzing and constructing quasi-cyclic low-density parity-check codes, *Information Theory and Applications Workshop*, page(s): 1-8, 2011.

[9] C.E.Shannon, A mathematical theory of communication, Bell Syst. Tech., 1948, vol.27: 379-423, 623-656.

[10] Yu Kou, Shu Lin and Marc P. C.Fossorier, Low-density parity-check codes based on finite geometries a rediscovery and new results, *IEEE Trans. on Information Theory*, 47(7): 2711 – 2736, 2001.

[11] Shu Lin, Daniel J. Costello, Jr, Error Control Coding, Second Edition, ISBN 978-7-111-20804-4.

[12] CCSDS131.1-O-2.2007.Low Density Parity Check Codes For Use In Near-Earth And Deep-Space Applications [S].Washington, DC, USA, CCSDS.