PCM coding of the FPGA design of Repeaters

JI CHAO LIU [1, A], JU WANG [1, B], WEI JUAN ZHANG [1, C] , KUN LI [1]

[1]Yanching Institute of Technology, Yanjiao, 065201, China

[a]email 158747917@qq.com, [b]email jubin-2006@163.com, [c]email zwj1021@126.com

Keywords: PCM, Repeater, FPGA, Digital communication.

Abstract. This document explains and demonstrates how to prepare your camera-ready manuscript for Trans Tech Publications. Digital communication is a very important technology in modern multimedia technology, it makes up the defect analog communication many, many, but in digital communication, signal attenuation is hampered by long distance transmission, channel or line repeater can make by the number of fixed into a vast quantity and random service path. In this paper, starting from the principle of PCM to relay, for the purpose of using PCM coding on the FPGA design.

Introduction

PCM is a kind of modern theory of relatively simple and perfect communication code, it is the continuous stimulation signal transform into discrete in time and amplitude, and converted to code transmission. Its more than digital signal in long distance transmission through and noise and not cumulative, which makes the communication system of high efficiency, high reliability and high secrecy [1]. Due to the above advantages, this paper by using FPGA, and now the mainstream used in the design of digital communication repeater based on PCM coding.

System Analysis

Pulse Code Modulation for PCM (Pulse Code Modulation), it is one of a variety of encoding of digital communication. The main is to analog signal according to certain interval sampling, this will be after discrimination integer sampling values quantitatively, and then to quantify the value of the represented by binary code [2]. Foam sampling is the process of the bandwidth is greater than 2 times more than analog signal bandwidth of frequency value extracted sample value, makes the analog signal into the process of discrimination of the signal in time. So if you want to restore to become the original analog signal, only the sampling signal detection and smooth filtering, which is the important process of analog signals into digital signals, and its precision depends on the size of the sampling frequency. Although in time after sampling signal is discrete digital signal, but in its amplitude is still analog signal sampling signal within a certain range of values. Value more than normal for the limited its samples, the sample values expressed in digital code, must adopt the method of decimal "rounded" were classified, the sample value is the integer, make certain value range of sample values into a finite number of values. This is the process of quantification; its accuracy depends on number of sample values. Coding is the quantification of sampling signal from decimal code conversion to determine, in the form of binary code needed for the process[3].

Repeater (RP repeater) used for two-way receiver signal between two network nodes, is a kind of important device connected to the line, the bitwise in the physical transmission of digital information, to copy, adjustment and amplification of signal, extend the length of the communication network. On the long road for signal transmission, power attenuation, if attenuation to a certain degree can cause signal distortion, bit error rate has increased dramatically, so you need to have Repeaters, its node in transmission network for physical connections, and a decrease of digital signal is amplified and make the digital signal can keep the same as the original digital signal. Although theoretically can know, repeater can infinite set up, which means that the transmission network can be unlimited extension. But in fact it is not possible, the signal after a number of Repeaters, can cause substantial delay time

only a finite number of connections, with the network transmission speed, for normal and effective work, lest cause the network transfer delay and failure.

As shown in Figure 1,Field Programmable Gate Array (FPGA) (Field Programmable Gate Array) is referred to as the FPGA, it is suitable for application-specific integrated circuit (ASIC) Field of a half a custom circuit, and it overcomes the original various Programmable device Gate a limited number of faults, and solve the custom circuit fixed trouble. Logic Cell Array FPGA using LCA (Logic Cell Array), and its internal include Configurable Logic module CLB (Configurable Logic Block), Output, Input module IOB (Input Output Block) and the internal connections (Interconnect) three parts [4]. Mainstream FPGA is still on the market at present is to use a lookup table of technology, but has greatly exceeded the basic properties of the original version, and integration of the common function of ASIC hardcore module. Its chip is mainly composed of six parts: the programmable input/output unit (IOB), configurable logic block (CLB), digital clock management module (DCM), embedded block RAM (BRAM), rich resources of wiring, the underlying inline function unit and embedded special hardcore.

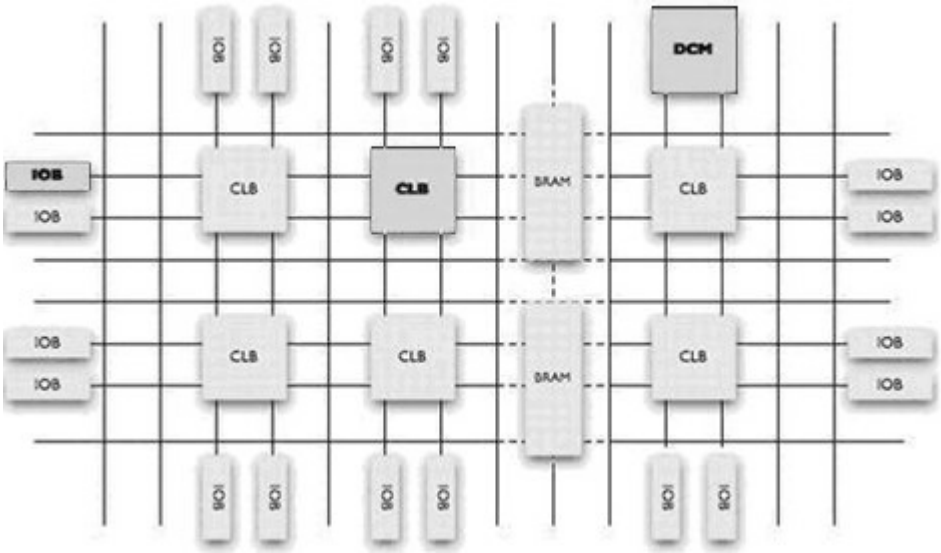

Fig.1 FPGA chip

In order to can be effective, reliable and comprehensive implementation of the required functionality, based on the large-scale programmable logic device (PLD) as control unit, and USES the launched by Mitel company can produce and deal with the integrated device PCM30/32 signal - MT9075 chip as the core of the repeater device, it synthesized PCM30/32 into the frame, and linear interface unit (LIU) and link controller (LRC England, not only have the function of the clock, interrupt and processing are synchronous, and error protection, the echo signal, the CAS signaling and CCS signal processing, and other functions. The chip provides parallel interface can be easily connected to large-scale programmable logic devices, and related to the chip internal register read and write operations, in order to realize the signal of transmission lines and to control and processing instructions. According to the demand, as PCM line repeater[5], realizes the PCM code switching and data exchange, the designed device should first satisfy the input and output type should be as the HDB3 code, and the external output clock should be 2048 KHZ, in order to meet the transmission frequency of PCM, in addition to the above basic functions, can also join the input test and display, such as the output Settings, frame loss warning, all for the "0" (may be no signal[6], HDB3 code does not allow for the fourth straight "0") warnings and full of "1" (HDB3 code for + 1, 1 appear alternately[7], if four straight "0", add B and V and adjustment and appear with a + 1 or - 1) as a warning[8].

Module Design

PCM coding relay design based on FPGA, based on the FPGA as the core unit, MT9075, 6 b595 as aided design, on the other devices such as design method is as follows:

The FPGA design.FPGA unit circuit mainly includes configuration circuit and the design of the I/O interface unit, configuration of circuit is mainly used for the logic code download to the target chip, I/O interface circuit is mainly used for control of the peripheral circuit. The FPGA using EP1C6Q240 Cyclone series chip of Altera company. It can realize frame synchronization and data merging of complicated logic function, and the FPGA configuration of the device USES is EPCS4, low prices, low in system programmable (ISP) and Flash memory access, the chip has a capacity of 5980 logical unit, and have as many as 92160 RAM, kernel voltage of 1.5 V, the voltage of 3.3 V I/O interface. Theoretically MT9075 work clock and FPGA internal logic of a clock to complete synchronization, and because MT9075 chip need 20 MHZ as the normal work of the external system clock, in order to avoid the emergence of asynchronous logic need to choose the internal PLL frequency multiplier and implementation to adjust the design method of the synchronous clock, this is called directly internal phase-locked loop macro module, it can achieve its simple design, only need according to clew, sets the input clock frequency and the need of the output clock frequency can be achieved. FPGA crystals will produce 10 MHZ external clock, from selection module of phase-locked loop input clock input pin, after frequency multiplication phase-locked loop into, can output from the output pin of 20 MHZ outside the system clock, it becomes out of synchronization. Which the output clock is divided into three road, implementation requirements of use, which is for the use of relay control logic module, all the way to 6 b595, another way is to supply MT9075 control logic module is used, and all the way for direct output, provide external MT9075 system clock.

The original relay control is implemented using 6 b595 chip, its function is used to control the string and transformation. Six b595 sent upon receipt of the FPGA chip to serial control string signal, after the chip internal control switch, the module of parallel output to connect. Its most began to enter the first level is composed of 8 D flip-flop D flip-flop, under the control of data is on the rise along the serial input from SDI pins, and latches to 2 D after the trigger for a second latch, under ST setting signal control delay and output, and end with her through the door, the output of the DMOS gate level g, gate level g for MOS tube conduction control side, the high grade only when the grid g as electricity at ordinary times, the MOS grade pipe leakage source level s and D to conduction, to make the device work, if g gate level is low level, the field effect tube will be in by the state, the relay is the default state.

MT9075 interface design. MT9075 and other functions, mainly introduces the design of sending and receiving only here. Send the logical function is one of the main logic of the control logic of MT9075, here sent after implementation of the PCM frame format conversion, the function that sends data of each time slot will be in accordance with the PCM30/32 frame format for encoding, and then the serial input from MT9075 DSTi pin. One of the clock signal can be used for serial output and a string of conversion data, the clock signal will be used in 32 latch distributor of sampling signals, and parallel and serial output of data need to input the data synchronization, need for sampling signal. Logic function is contrary to send logic functions, the function is mainly from MT9075 chip serial output data stream according to the PCM30/32 encapsulate frame format, namely the data conversion of serial parallel data, store again , after receiving the can module, string and conversion module will from MT9075 chip output data according to PCM30/32 converted into 8 bits parallel data frame format, and then after the output latch is connected to the level of latch. Highest in nine surprising parity bit, low 8 bits of data bits. Receiving module is mainly composed of the several sub-modules: receive enabled modules; String and conversion module; Odd-even frames the produce module; Receiving time slot gating module; Storage module.

Other Modules. In addition to the above module, and input/output interface circuit module, it should include: the loop control circuit, 2048 KHZ output clock driver and isolation circuit, interface circuit protection and relay interface transformer isolation circuit four parts, in the design of hardware, power supply and the point pressure, must pay attention to the parts of the adjustment of the input and output impedance and grounding of good sex and isolation circuit. Therefore, input and output interface of I/O interface can be designed by interface with isolation transformers, relay and protection circuit. And the power supply circuit mainly by the backend FPGA parts, peripheral interface chip as well as the front-end interface composed of three parts. The final conversion circuit

with 6 b595 can finish, so that can meet the needs of the current design, also can simplify the circuit.

Conclusion

First introduced in this paper, the PCM coding, repeater and FPGA, and then USES the large-scale programmable logic devices to design realize the design of the PCM coding repeater, choose FPGA as the core, with other devices such as MT9075 and 6 b595, used to implement the PCM coding relay design, modular design way, easy to understand, and ease of replacement and repair of the device. With the development of modernization of law, analog communication though there is no alternative, but digital communication will be developed toward the direction of the higher data transfer rate will also be increased because of the network and communication technology and greatly improved, and will gradually appear all sorts of new type of optimization code and highly integrated device. By way of design, presented in this paper to a higher level of integration, better encoding, continue to develop on a shorter delay time.

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