A Wireless Image Transmission System Based on Visible Light Communication

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Abstract. In this letter, a wireless image transmission system is proposed and presented based on the visible light communication (VLC). This system consists of OV7670 image acquisition module, STM32, encoding module based on FPGA, modulation driving circuit and LED. IPPM, which has advantages of high average transmit power and large SNR, is firstly proposed for applying in image transmission system. Theoretical design and experiment verification are carried out. The agreement between the simulated and measured results is good. The proposed image transmission system can improve the communication capacity and decrease the bit error ratio. It is suitable for the applications of large-capacity and high-speed commutation.

Introduction

As the new generation of solid-state light source, white LEDs have advantages of long life, low energy consumption, environmental protection, etc. Therefore, applications of white LEDs have a rapid development in the field of in the illumination, with the development and improvement of white LEDs lighting technology. The switching frequency of LEDs is high and easy to realize high-speed modulation. So it can be realized wireless visible lighting communication (VLC) at the same time of illumination. VLC technology has the potential to research be a robust candidate for the overcrowded spectrum of radio frequency today. This fast-developing technology has several benefits including no electro-magnetic interference, no electromagnetic radiation, good privacy and energy conservation, etc. Camera module is consisted of OV7670 and FIFO chip to realize image acquisition. IPPM is adopted here which has advantages of high average transmit power and large SNR. STM32 is used in the transmitter for reading image data and sending the data by the modulation circuit. STM32 is used in the receiver for reading the data of decoder circuit. Then, the image is displayed on a 3.2-inch TFT.

Transmitter design

The block diagram of the proposed transmitter shown in Fig. 1 consists of OV7670 image acquisition module, STM32, encoding module based on FPGA, modulation driving circuit and LED. Image from camera is captured by OV7670 module which can holds the high image data in the FIFO chip. The pixel clock of the OV7670 is 24MHz which is difficult to capture using STM32. At the same time, lots of CPU are used. Therefore, FIFO chip is introduced into this model due to much better advantage of reading complete image information from camera at real time. Then STM32 reads the image information form the FIFO corresponding register through I/O at low speed. And the image information is sent to FPGA module. Finally, the image for comparing with the image of receiver can

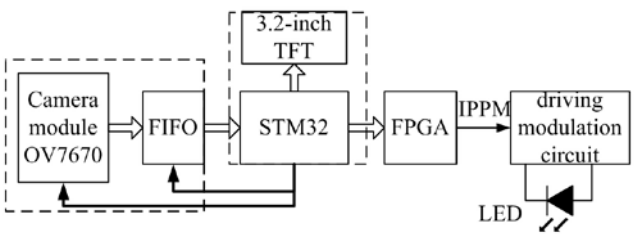

Figure 1. The block diagram of transmitter

be successfully displayed on the 3.2-inch TFT.

IPPM is inversion of pulse position modulation (PPM). PPM based on intensity modulation with direct detection, is used in VLC systems. However, In IPPM, information bits are encoded into an optical pulse and are distinguished by the pulse position.

Fig. 2 shows the frame structure for 16-IPPM and comparison of 16-PPM.T_s is the width of the code element. T_i and T_g are the data frame and the protection section, respectively. Bandwidth is estimated by the major lobe of power density. The width of the optical pulse slot is narrow. Therefore, the signal bandwidth through the reciprocal of T_s can be estimated by:

$$B_{16-IPPM} = \frac{1}{Ts} \bullet \frac{2^M + N}{M}. \tag{1}$$

M=4 and N=4 in Eq.1, the information rate is:

$$R_b = \frac{M}{(2^M + N) \bullet Ts}. \tag{2}$$

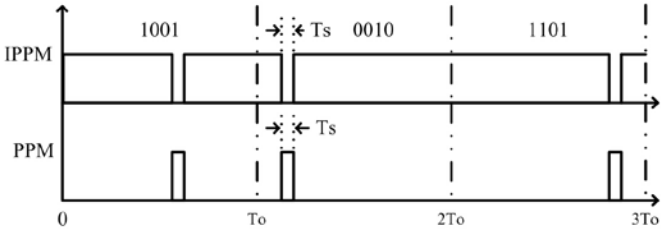

Figure 2. Comparison of frame structure between IPPM and PPM.

STM32 sends the information to FPGA through parallel I/O. FPGA holds the information in buffer in the first half cycle of each frame and sends the information into comparator for comparing with the value of the counter. The pulse former produce a narrow pulse When the results of the comparison are equal. Coding is done in IPPM signal.

The modulation circuit is shown in Fig. 3. The circuit consists of the DC supply circuit based on LT3755 and the signal amplifier circuit. LT3755 is DC/DC controllers designed to operate as a constant-current source for driving high current LEDs.

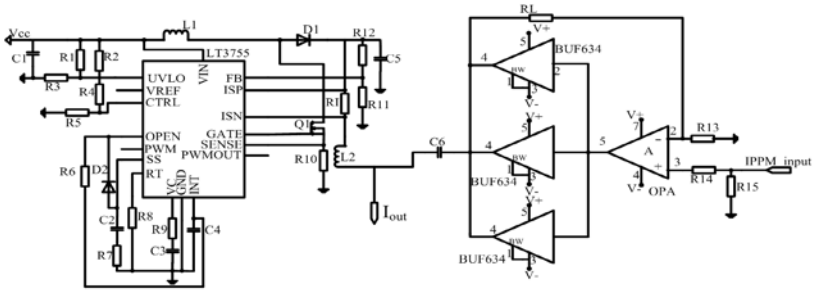

Figure 3. Modulation driving circuit.

The fixed frequency, current mode architecture results in stable operation over a wide range of supply and output voltages and the ripple current of bias DC is small. So the bit error rate (BER) performance of this VLC system is reduced. Once the selecting of the value of resistors R1, R11 and R12, the value of the DC bias will be determined.

The IPPM output of the FPGA module is a low current. Combining an operational amplifier and the high-speed buffer BUF634 located in its feedback loop is proposed. Here, the operational amplifier is responsible for precision. The necessary current is provided by the BUF634. This configuration compensates the buffer's internal resistance and the output resistance of the entire circuit is close to zero. So the circuit contains three BUF634 in parallel in order to achieve current amplification.

Receiver design

The receiver circuit is shown in Fig. 4. It is consisted of PIN, amplifier circuit, FPGA decoding module, STM32 and 3.2-inch TFT. The directly modulated optical signal is received by the PIN photodiode. The current signal is amplified by using a preamplifier and a two-stage limiting amplifier shown in Fig. 5. The current signal is converted into the voltage signal and is decoded in FPGA module. The image information is obtained by STM32 and is displayed on a 3.2-inch TFT. A1 is an high gain bandwidth, low distortion, voltage-feedback op amp, with a low voltage noise. The transimpedance amplifier which is composed of A1 is a current to voltage converter and amplifies the current output of PIN to a usable voltage. The two-stage limiting amplifier amplifies the IPPM voltage signal and makes it stable for better quality of IPPM decoding.

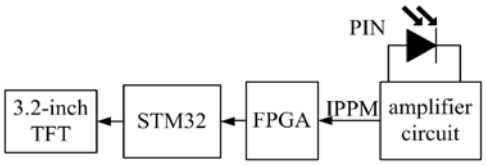

Figure 4. The block diagram of receiver

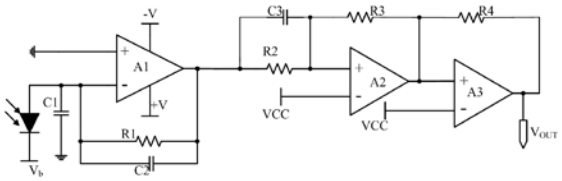

Figure 5. The receiving circuit.

Experimental results

Fig. 6 shows the VLC system experimental link. A bi-convex lens is used and the link operates over a distance of 3m with a single 10W white LED. The Bias dc is 360mA and the IPPM signal peak current is 100mA, the modulation depth M is:

$$M = \Delta I / 2I_b \quad . \tag{3}$$

M=13.89% can be determined by Eq.3. It is a suitable value for this VLC system, the higher value of M, the easier optical signal to detect, but excessive value may decreases modulation bandwidth of system.

The width of the code element Ts is set to 340ns, Fig. 7. shows the waveform of IPPM signal output of FPGA module in transmitter and the IPPM signal output of limiting amplifier in receiver.

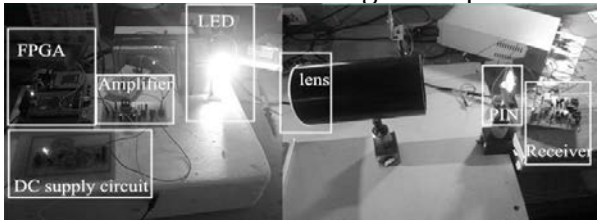

Figure 6. VLC system experiment link.

The good transmitted waveform shows the modulation capability of modulation circuit. The waveform is a delay Δt=550ns in receiver. The IPPM signal is an ideal output after the preamplifier and limiting amplifier. From Eq.2, the information rate is R_b=588Kbps. Compared with the images on the TFT, image transmission is perfectly realized.

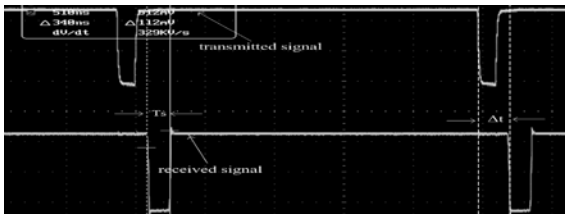

Figure 7. The signal waveform.

Summary

In this letter, a VLC system is designed which is successfully implemented for image transmission. The reliability of the VLC system is demonstrated using IPPM and the experimental results. The LED driving modulation circuit has a good luminoue efficiency and high power. This system also has a good ability for illumination and the communication distance of the system satisfy indoor lighting's demand. Therefore, it can be suitable for many potential applications. Furthermore, an idle pattern is inserted in the protection section to realize the predigestion of the IPPM demodulator circuit. Further work will be concerned with the higher information transfer rate and higher power efficiency.

Acknowledgements

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