

Die to Package Interconnection Materials and Technologies

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Abstract. This article introduced the technologies of die to package .these mainly including wire bonding(WB),tape-automated bonding(TAB),and flip chip(FC).the most common wire bonding technique is ball bonding. This is the foundation of the others .at the end parts, the paper illustrated the new interconnection technology –TSV, it bring us from 2D to 3D interconnection times.

Wire bonding

Wire bonding is the method of making interconnections between an integrated circuit (IC) or other semiconductor device and its packaging during semiconductor device fabrication. Although less common, wire bonding can be used to connect an IC to other electronics or to connect from one PCB to another. Wire bonding is generally considered the most cost-effective and flexible interconnect technology, and is used to assemble the vast majority of semiconductor packages.

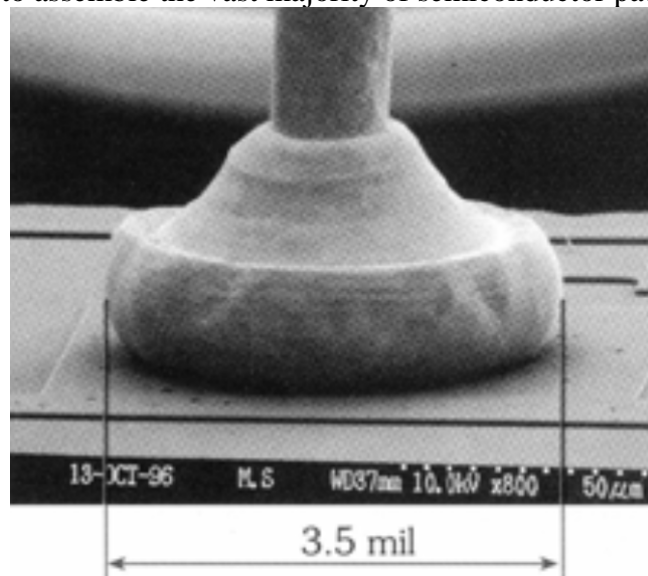


Fig.1 The first bonding point's picture

Bonding Materials

Bond wires usually consist of one of the following materials: Aluminum, Copper, Silver, and Gold. Wire diameters start at 15 μm and can be up to several hundred micrometres for high-powered applications.

The wire bonding industry is transitioning from gold to copper.[1][2] This change has been instigated by the rising cost of gold and the comparatively stable, and much lower, cost of copper. While possessing higher thermal and electrical conductivity than gold, copper had previously been seen as less reliable due to its hardness and susceptibility to corrosion. By 2015, it is expected that more than a third of all wire bonding machines in use will be set up for copper. [3]

Copper wire has become one of the preferred materials for wire bonding interconnects in many semiconductor and microelectronic applications. Copper is used for fine wire ball bonding in sizes up

to 0.003 inch (75 micrometres). Copper wire has the ability of being used at smaller diameters providing the same performance as gold without the high material cost.[4]

Copper wire up to 0.010 inch (250 micrometres) can be successfully wedge bonded with the proper set-up parameters. Large diameter copper wire can and does replace aluminum wire where high current carrying capacity is needed or where there are problems with complex geometry. Annealing and process steps used by manufacturers enhance the ability to use large diameter copper wire to wedge bond to silicon without damage occurring to the die.[4]

Copper wire does pose some challenges in that it is harder than both gold and aluminum, so bonding parameters must be kept under tight control. The formation of oxides is inherent with this material, so storage and shelf life are issues that must be considered. Special packaging is required in order to protect copper wire and achieve a longer shelf life.[4] Palladium coated copper wire is a common alternative which has shown significant resistance to corrosion, albeit at a higher cost and hardness than pure copper, though still less than gold. During the fabrication of wire bonds, copper wire, as well as its plated varieties, must be worked in the presence of forming gas [95% nitrogen and 5% hydrogen] or a similar anoxic gas in order to prevent corrosion. A method for coping with copper's relative hardness is the use of high purity [5N+] varieties. [5]

Pure gold wire doped with controlled amounts of beryllium and other elements is normally used for ball bonding. This process brings together the two materials that are to be bonded using heat, pressure and ultrasonic energy referred to as thermosonic bonding. The most common approach in thermosonic bonding is to ball-bond to the chip, then stitch-bond to the substrate. Very tight controls during processing enhance looping characteristics and eliminate sagging.

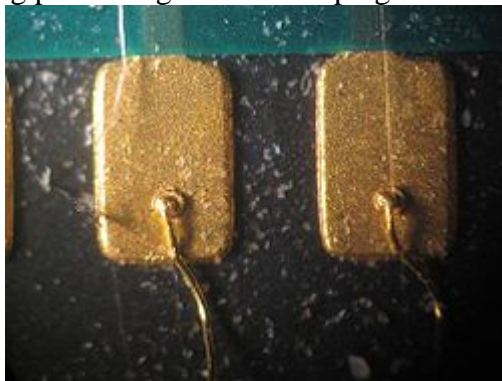


Fig.2 Gold wire ball-bonded to a gold contact pad

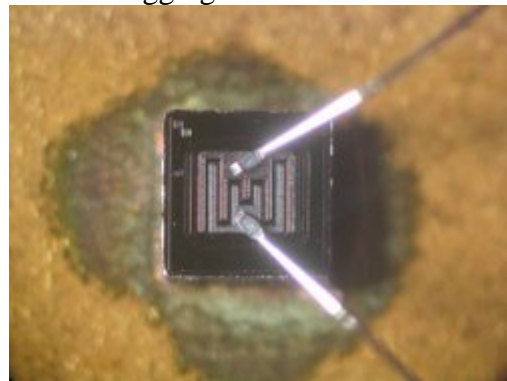


Fig.3 Aluminium wires wedge-bonded to a transistor die

Junction size, bond strength and conductivity requirements typically determine the most suitable wire size for a specific wire bonding application. Typical manufacturers make gold wire in diameters from 0.0005 inch (12.5 micrometers) and larger. Production tolerance on gold wire diameter is $\pm 3\%$. [5]

Alloyed aluminum wires are generally preferred to pure aluminum wire except in high-current devices because of greater drawing ease to fine sizes and higher pull-test strengths in finished devices. Pure aluminum and 0.5% magnesium-aluminum are most commonly used in sizes larger than 0.004 inch.

All-aluminum systems in semiconductor fabrication eliminate the "purple plague" (brittle gold-aluminum intermetallic compound) sometimes associated with pure gold bonding wire. Aluminum is particularly suitable for ultrasonic bonding.

In order to assure that high quality bonds can be obtained at high production speeds, special controls are used in the manufacture of 1% silicon-aluminum wire. One of the most important characteristics of high grade bonding wire of this type is homogeneity of the alloy system. Homogeneity is given special attention during the manufacturing process. Microscopic checks of the alloy structure of finished lots of 1% silicon-aluminum wire are performed routinely. Processing also is carried out under conditions which yield the ultimate in surface cleanliness and smooth finish and permits entirely snag-free de-reeling.[6]

Tape-automated bonding

The process was invented by Frances Hugle. Historically, TAB was created as an alternative to wire bonding and finds common use by manufacturers in LCD display driver circuits.[9]

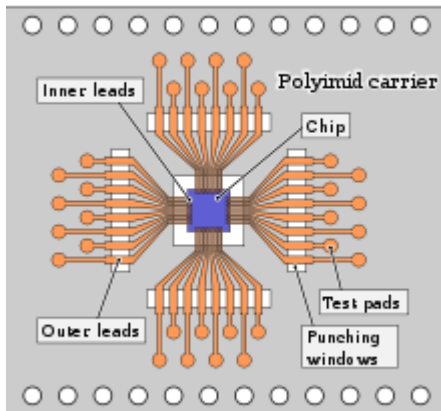


Fig.4 Chip attaching on TAB

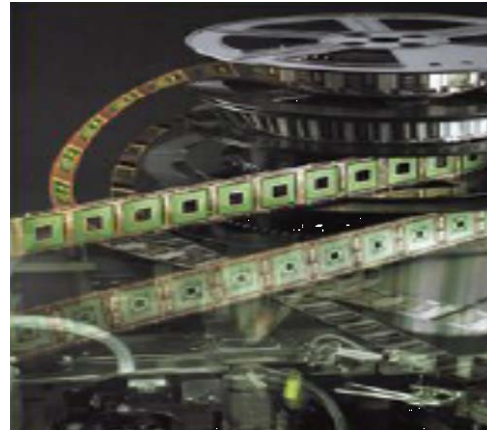


Fig.5 TAB'S film

Tape-automated bonding (TAB) is a process that places bare integrated circuits onto a printed circuit board (PCB) by attaching them to fine conductors in a polyamide or polyimide film, thus providing a means to directly connect to external circuits.

TAB Process. The tape-automated bonding process places bare integrated circuits onto a printed circuit board. The mounting is done such that the bonding sites of the die, usually in the form of bumps or balls made of gold or solder, are connected to fine conductors on the tape, which provide the means of connecting the die to the package or directly to external circuits[17]. Sometimes the tape on which the die is bonded already contains the actual application circuit of the die.[7] The film is moved to the target location, and the leads are cut and soldered as necessary. The bare chip may then be encapsulated ("glob topped") with epoxy or plastic.[8]

Standards. Standard sizes for polyimide tapes include widths of 35 mm, 45 mm, and 70 mm and thicknesses between 50 to 100 micrometers. Since the tape is in the form of a roll, the length of the circuit is measured in terms of sprocket pitches, with each sprocket pitch measuring about 4.75mm. Thus, a circuit size of 16 pitches is about 76mm long.[7]

Flip chip

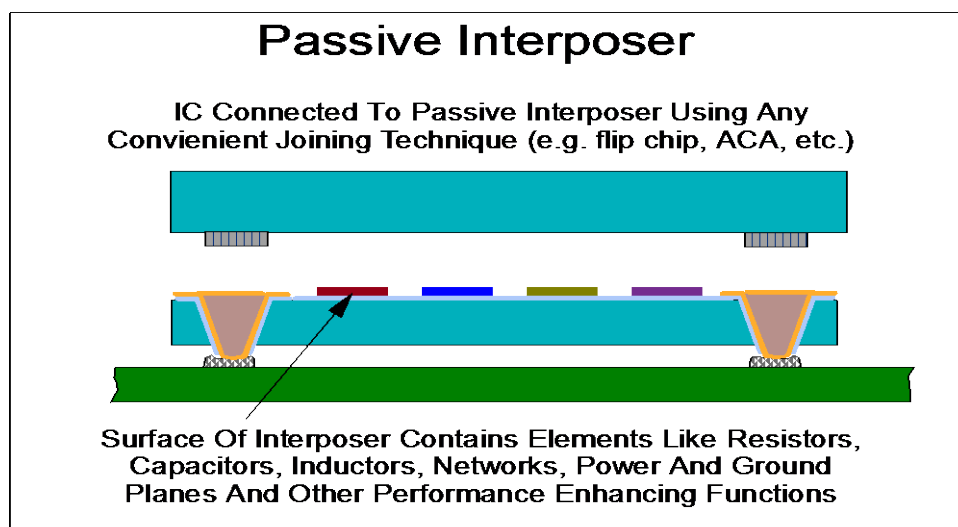


Fig.6 FC connection product

The process was originally introduced commercially by IBM in the 1960s for individual transistors and diodes packaged for use in their mainframe systems.[10] DEC followed IBM's lead, but was unable to achieve the quality they demanded, and eventually gave up on the concept. It was pursued once again in the mid-90s for the Alpha product line, but then abandoned due to the fragmentation of

the company and subsequent sale to Compaq. In the 1970s it was taken up by Delco Electronics, and has since become very common in automotive applications.

Flip chip, also known as controlled collapse chip connection or its acronym, C4, is a method for interconnecting semiconductor devices, such as IC chips and micro electro mechanical systems (MEMS), to external circuitry with solder bumps that have been deposited onto the chip pads. The solder bumps are deposited on the chip pads on the top side of the wafer during the final wafer processing step.

In order to mount the chip to external circuitry (e.g., a circuit board or another chip or wafer), it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and then the solder is reflowed to complete the interconnect. This is in contrast to wire bonding, in which the chip is mounted upright and wires are used to interconnect the chip pads to external circuitry.

Process steps

Integrated circuits are created on the wafer

Pads are metalized on the surface of the chips

Solder dots are deposited on each of the pads

Chips are cut

Chips are flipped and positioned so that the solder balls are facing the connectors on the external circuitry

Solder balls are then remelted (typically using hot air reflow)

Mounted chip is “underfilled” using an electrically-insulating adhesive[11]

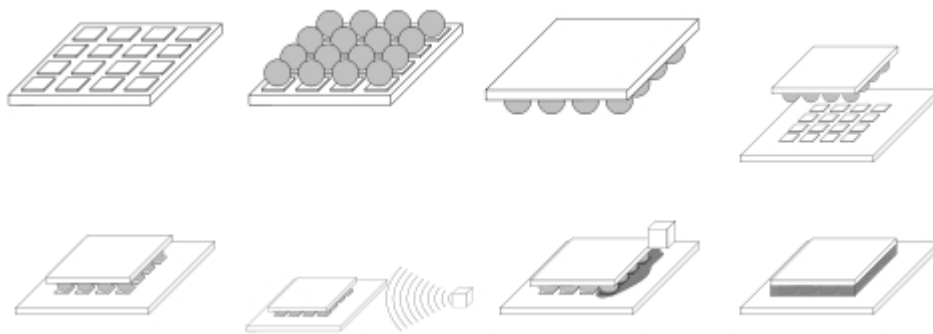


Fig.7 Flip chip technologies

Processing a flip chip is similar to conventional IC fabrication, with a few additional steps.[12] Near the end of the manufacturing process, the attachment pads are metalized to make them more receptive to solder. This typically consists of several treatments. A small dot of solder is then deposited on each metalized pad. The chips are then cut out of the wafer as normal.

To attach the flip chip into a circuit, the chip is inverted to bring the solder dots down onto connectors on the underlying electronics or circuit board. The solder is then re-melted to produce an electrical connection, typically using a Thermosonic bonding or alternatively reflow solder process. This also leaves a small space between the chip's circuitry and the underlying mounting. In most cases an electrically-insulating adhesive is then "underfilled" to provide a stronger mechanical connection, provide a heat bridge, and to ensure the solder joints are not stressed due to differential heating of the chip and the rest of the system. The underfill distributes the thermal expansion mismatch between the chip and the board, preventing stress concentration in the solder joints which would lead to premature failure. [13]

Recently, high-speed mounting methods evolved through cooperation between Reel Service Ltd. And Siemens AG in the development of a high speed mounting tape knew as 'MicroTape.' [14]. By adding a tape-and-reel process into the assembly methodology, placement at high speed is possible, achieving a 99.90% pick rate and a placement rate of 21,000 cph (components per hour), using standard PCB assembly equipment.

Advantages. The resulting completed flip chip assembly is much smaller than a traditional carrier-based system; the chip sits directly on the circuit board, and is much smaller than the carrier both in area and height. The short wires greatly reduce inductance, allowing higher-speed signals, and also conduct heat better.

Disadvantages. Flip chips have several disadvantages. The lack of a carrier means they are not suitable for easy replacement, or manual installation. They also require very flat surfaces to mount to, which is not always easy to arrange, or sometimes difficult to maintain as the boards heat and cool. Also, the short connections are very stiff, so the thermal expansion of the chip must be matched to the supporting board or the connections can crack.[15] The underfill material acts as an intermediate between the difference in CTE of the chip and board.

Flip chips have recently gained popularity among manufacturers of cell phones, pagers and other small electronics where the size savings are valuable.[citation needed]

Through-silicon via

The concept of Through-Silicon Via appeared in late 1990s. The co-founder and current CEO of ALLVIA, Inc. coined the term "through-silicon via" in 1997 as part of his original business plan. From the beginning, the vision of the business plan was to create a through silicon interconnect since these would offer significant performance improvements over wirebonds.

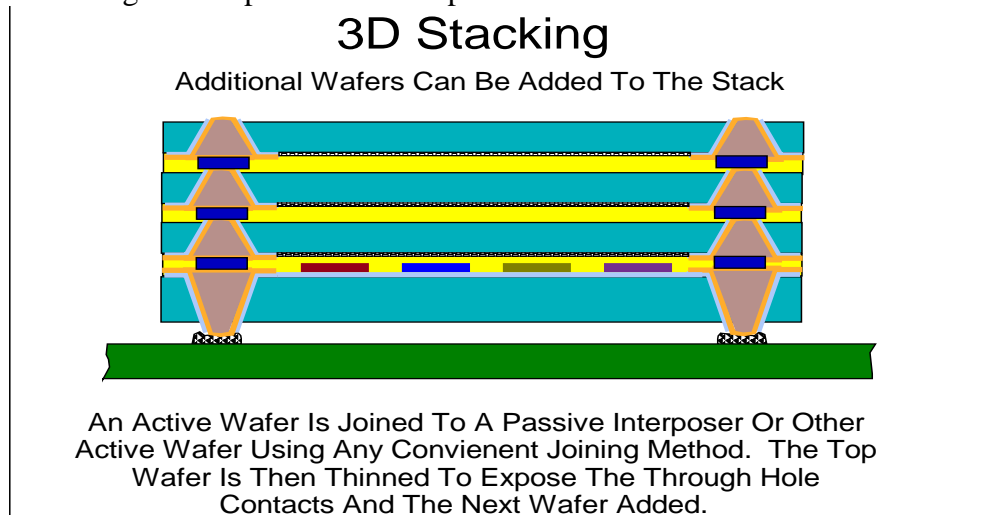


Fig.8 3Dpacking

The article “Moore’s Law – The Z Dimension” was published in Solid State Technology magazine in January 2000. This article outlined the roadmap of the TSV development as a transition from 2.5-D chip stacking to wafer level stacking in the future. In one of the sections titled Through-Silicon Vias, Dr. Sergey Savastiouk wrote: “Investment in technologies that provide both wafer-level vertical miniaturization (wafer thinning) and preparation for vertical integration (through silicon vias) makes good sense.” He continued: “by removing the arbitrary 2-D conceptual barrier associated with Moore’s Law, we can open up a new dimension in ease of design, test, and manufacturing of IC packages. When we need it the most – for portable computing, memory cards, smart cards, cellular phones, and other uses – we can follow Moore’s Law into the Z dimension.” It was the first time the term "through-silicon via" was used in a technical publication.

In electronic engineering, a through-silicon via (TSV) is a vertical electrical connection (via)(Vertical Interconnect Access) passing completely through a silicon wafer or die. TSVs are a high performance technique used to create 3D packages and 3D integrated circuits, compared to alternatives such as package-on-package, because the density of the vias is substantially higher, and because the length of the connections is shorter. [16]

Through Silicon Via (TSV) is an enabling technology that allows electrical connections to be formed through a silicon wafer or multi-wafer devices. Electrical connections through a silicon wafer allow for reduced die footprints and interlayer connectivity. When combined with Wafer Level

Packaging (WLP), TSVs minimize die size, allow conventional or flip-chip bonding, and help minimize cost of the final macroscale device.

Micralyne offers polysilicon TSV technology for custom prototyping and manufacturing. Connections between layers are created through etching via holes, selectively insulating, and filling with conductive polysilicon. This platform includes deep etched silicon trenches, isolation or grounding vias, polysilicon filling, and the option for integration in SOI wafer stacks. We would be pleased to discuss your MEMS TSV requirements, including aspect ratio, thickness, pitch, resistivity, and capacitance, geometry, and isolation resistance.

TSV technology in 3D packages. A 3D package (System in Package, Chip Stack MCM, etc.) contains two or more chips (integrated circuits) stacked vertically so that they occupy less space and/or have greater connectivity. An alternate type of 3D package can be found in IBM's Silicon Carrier Packaging Technology, where ICs are not stacked but a carrier substrate containing TSVs is used to connect multiple ICs together in a package. In most 3D packages, the stacked chips are wired together along their edges; this edge wiring slightly increases the length and width of the package and usually requires an extra "interposer" layer between the chips. In some new 3D packages, through-silicon vias replace edge wiring by creating vertical connections through the body of the chips. The resulting package has no added length or width. Because no interposer is required, a TSV 3D package can also be flatter than an edge-wired 3D package. [18] This TSV technique is sometimes also referred to as TSS (Through-Silicon Stacking or Thru-Silicon Stacking).

TSV technology in 3D ICs. A 3D integrated circuit (3D IC) is a single integrated circuit built by stacking silicon wafers and/or dies and interconnecting them vertically so that they behave as a single device. [19] By using TSV technology, 3D ICs can pack a great deal of functionality into a small "footprint." The different devices in the stack may be heterogeneous, e.g. combining CMOS logic, DRAM and III-V materials into a single IC. In addition, critical electrical paths through the device can be drastically shortened, leading to faster operation.

Fig.9 below shows a variety of vias from a scanning electron microscope. [18]

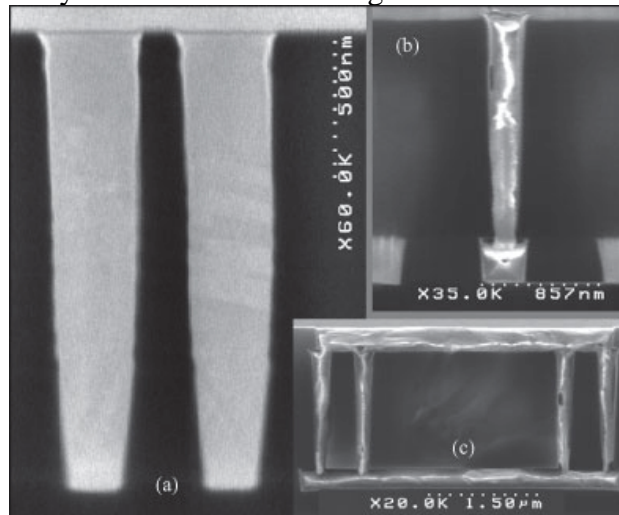


Fig.9 (a) Cross section of ~1.6µm high via, (b) cleaved SEM image of isolated via (c), cleaved SEM image of ~175nm diameter vias (Source: IBM)

As die size become more big and the feature size become more tiny, from WB to TSV ,we see the interconnection technology changed very fast. It had developed from 2D to 3D Times.

References

- [1] Mokhoff, Nicolas (March 26, 2012)."Red Micro Wire encapsulates wire bonding in glass".EE Times(San Francisco:ISSN0192-1541.OCLC56085045.Archived from the original on March 20, 2014. Retrieved March 20, 2014.
- [2] "Product Change Notification ".microchip.com.August29, 2013. Archived from the original on March 20, 2014. Retrieved March 20, 2014.

- [3] Chauhan, Preeti; Choubey, Anupam; Zhong, ZhaoWei; Pecht, Michael(2014). Copper Wire Bonding (PDF).NewYork:Springer.ISBN978-1-4614-5760-2.
- [4] "Copper Bonding Wire: ElectricalInterconnect Materials". from the original on March 20, 2014. Retrieved March 20, 2014.
- [5] "Gold Bonding Wire and Ribbon: WireforAutomaticBonders". From the original on March 20, 2014. Retrieved March 20, 2014.
- [6] "Aluminum Bonding Wire and Ribbon: Silicon Aluminum Wire, Aluminum Ribbon". Archived from the original Retrieved March 20, 2014.
- [7] TAB at Silicon Far East on-line.
- [8] Tape-Automated Bonding". Centre for High Performance Integrated Technologies and Systems (CHIPTEC). March 1997.
- [9] Tape Automated Bonding (TAB)". Advantest Europe Customer Newsletter. Advantest GmbH.
- [10] Information on <http://wikipedia.Solder Bump Flip Chip>
- [11] Venkat Nandivada. "Enhance Electronic Performance with Epoxy Compounds". Design World. 2013.
- [12] Demerjian, Charlie (2008-12-17), Nvidia chips show underfill problems, The Inquirer, retrieved 2009-01-30
- [13] George Riley, Introduction to Flip Chip: What, Why, How, Flipchips.com October 2000.
- [14] Information on <http://realworldtech.com/page.cfm?ArticleID=RWT050207213241>
- [15] Information on <http://www.appliedmaterials.com/technologies/library/producer-avila-pecvd>
- [16] Information on http://www.businesswire.com/portal/site/appliedmaterials/permalink/?dmViewId=news_view&newsId=20100712005576&newsLang=en
- [17] Electronic packing technology and materials, ISBN978-7-03-031485-7, 2011-08, P.20-22.
- [18] 3D Integration: A Revolution in Design, May 2, 2007 by Euronymous.