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Impact of Defects Caused by Hot Charge Carriers on the Digital VLSI Parameters

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***Abstract* – The problem of establishing a contact between degradation at the instrument and the circuit levels while designing very large scale integrated circuits (VLSI) is of a great interest. Instrument and circuits sensitivity to the effects conded by hot carriers is different, which is determined by a large number of factors. Hot carriers generated at the boundary cause a charge, which causes a change in the electric field and carrier mobility in the channel, with the result that the device degrades non-uniformly. Instrument degradation parameters were used in the SPICE instrument modeling program to assess degradation caused by hot carriers. For the initial and exposed n-channel MIS transistor, using the SUXES program, the parameters of the model that characterizes the deterioration was determined. The results of the study show that for VLSI, containing mainly inverter and valve circuits, the degradation of the switching period from one logical value to another in the transmitting valves will be a decisive effect in the general characteristic of the circuits' switching period.**

Keywords – degradation; transistor; hot carriers; reliability; instrument modeling; impact ionization.

I. INTRODUCTION

With the transition to the very large scale integrated circuits (VLSI) manufacture using MIS technology, it is extremely relevant to establish the connection between degradation at the instrument level and at the circuit level [1–4]. Instrument and circuits sensitivity to the effects conded by hot carriers is different for several reasons [5, 6]: the different hot electrons' severity of exposure to transistors included in the circuit due to their difference in the dynamic waveform; transistors influence on the circuit's output characteristics in varying degrees; circuit differently sensitive to the same degree of change in the characteristic of the transistor depending on the type of the circuit itself.

Hot carriers generated at the boundary cause a charge, which causes a change in the electric field and carrier mobility in the channel, with the result that the device degrades non-uniformly [7–10].

II. METHODS AND MATERIALS

In the study, we measured substrate and drain electrical current measurement that were stored in the computer memory during the entire time when the voltage was applied to the device. The computer defined the values of these currents and, at each exposure period, adjusted the values of the voltages on the drain and the gate so as to ensure the connection constancy between the currents of the substrate and the drain during the research.

The degradation parameters for each instrument were determined based on a set of factors. Then these degradation parameters were put into the SPICE instrument modeling program in order to evaluate the parameters of the circuit after degradation caused by hot electrons. Based on the experimental and educated post-exposure estimates, the model parameters characterizing the instrument aging are chosen for the initial and exposed standard n-channel MOS transistor dependencies using the SUXES program: flat bands voltage, carrier mobility variations in the channel and lower barrier height caused by drain current. Calculated on the basis of this model, the values of the substrate current at different gate-drain voltage magnitude correspond to the experimental values.

To assess the changes in the scheme parameters, a CMDS structure was fabricated; the transistors port opening was 0.13 microns. To boost n-channel instruments degradation, they were manufactured without low-impurity regions of source and drain. The instrument-oxide thickness in the devices was 10 nm. To assess the passivation influencing on the degradation effects at the circuit level, two passivating coatings types were used: silicon nitride and phosphorosilicate glass (FSS) coating. The deterioration criterion was considered the ratio of the ring output frequency before and after exposure. This ratio change

at different values of exposure time and supply V_{DD} voltage power source is shown in Fig. one.

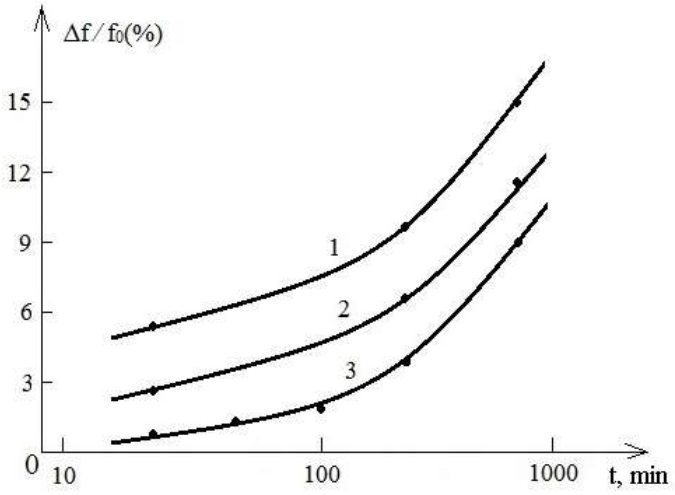

Fig. 1. The dependence of the ratio of the ring output frequency from the time of exposure, at different voltages (1- VDD= 3 V, 2- VDD= 3,5 V, 3- VDD= 4 V).

The smallest frequency change is observed at the highest voltage of the power source. This is due to the fact that at low voltages on the drain and gate the drain current degrades to a greater extent than at high voltage on the gate and the displacement of the drain area. Studies on the ring generators reliability, where the parameters were exposure time, power supply voltage, capacitive load and passivation technology, in all cases gave a coincidence of experimental and calculated data.

For the study at the circuit level, the following switching structures were chosen: CMDS-inverter (consisting of fan-out p-channel field transistor and a switching n-channel field transistor), CMDS-gate (consisting of an n-channel field transistor and p-channel field transistor) and n-MDP gate (consisting of n-channel field transistor). CMDS test crystal was formed by standard MDP technology on an insulating sapphire substrate. MIS field transistors, having in their composition switching valves, were characterized by effective values of the channel length and width of 0.18 and 2 μm, respectively. Inverter MDP field transistor had a p-channel width of 4 microns. The depth of the phosphorus-doped transitions was 100 nm, the gate-oxide thickness was 15 nm. The current was measured through the substrate, reflecting the development rate of the collision ionization process in the channel. Its value, determined experimentally, correlated with the change in the parameters of the circuits caused by the hot carriers' effects.

The indicator of the collision ionization rate in the channel is the current in the substrate. There is a correlation between the substrate current and the change in the parameters of the IC in the research process. The effect of defects caused by hot charge carriers on the parameters of the MIS field transistor is characterized by measuring the current-voltage characteristics with direct and reverse switching on of the instrument. These characteristics are directly related to the switching time of the digital IC. In order to determine the threshold voltage and the current voltage characteristic (CVC) slope the dependences of the drain current from the source-gate voltage (Vd = 0.1 V) were measured. When studying the digital ICs processing speed, a test signal with a frequency of 150 kHz was inputted and compared with the output signal, which was observed on an oscilloscope.

The substrate current occurrence in switching circuits is conded by the atoms collision ionization with hot electrons, which speed depends on the drain and gate potentials. These potentials may vary depending on the shape of the input signal and the type of load. One of the current substrate components is also the bias, evaluated by the pulses form. Unlike an inverter, n-MDP-conductive keys work symmetrically, i.e. the source and drain are swapped in the process of switching. Therefore, collision ionization processes occur in both the drain and source areas. The first current pulse of the substrate occurs when a logical unit passes through the key. Under these conditions, defects occur in the drain area. The second substrate current pulse occurs in conditions when a logical zero passes through the key. Under these conditions, defects arise in the source area. The potential on the input bus is less than the input voltage due to the threshold voltage drop between the gate and the n-MIS field transistor source. Consequently, the second substrate impulse current is much smaller than the first, and the hot charge carriers have a stronger effect on the drain area than on the source one. In the case of CMDS conductive keys, both pulses have the same amplitude conded by the p-MIS-field transistor participation in the potential transfer of the input signal to the output bus. This symmetric process becomes self-limiting, which significantly reduces the CMDS-keys processing speed degradation rate in comparison with n-MDP-keys.

The degradation caused by hot carriers is one of the factors that characterize the n-channel MDP BIS reliability. The direct connection between the MDP transistor degradation and the degradation of the integrated circuit based on it is difficult to identify, since the charge induced in nature by hot carriers is localized in the channel, so the device ceases to exhibit symmetrical characteristics at a constant current. The influence of this asymmetry on the switching VLSI characteristics has been studied.

As a characteristic of the degradation caused by hot carriers, we used the drain current dependence on the drain voltage (at a gate voltage of 5 V), measured both in the forward direction (i.e. with the same polarity as in the process of exposure to hot carriers), and in the opposite direction (with reverse polarity of the source and drain). These characteristics are also directly related to the switching time of the studied circuits. The dependences of the drain current on the gate voltage (at V_d = 0.1 V), which were measured in the forward direction, allows determining the threshold voltage and slope. When studying the degradation effect, a 300 kHz signal was applied to the circuit input and the output pulse form on the oscilloscope screen was analyzed; 5 V DC voltages were applied to the gate of the n-channel MDP field transistor. The voltage of the test signal was 5 V.

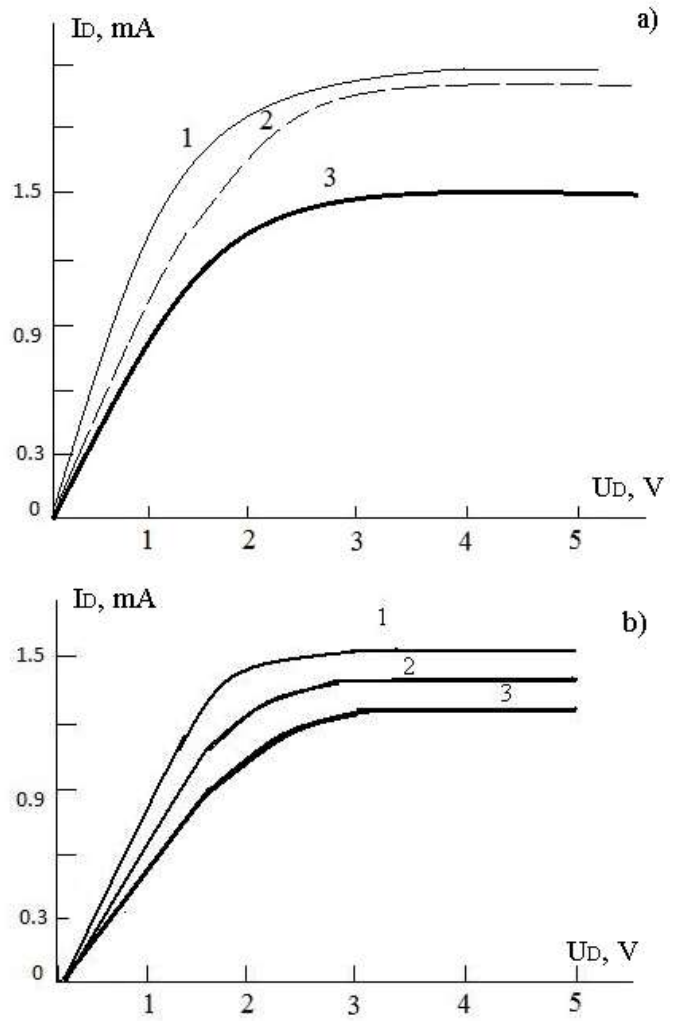

Fig. 2. Stock current voltage characteristic for n-MDP (a) and for CMDS (b) of the valve before impulse (1) and after it in the forward (2) and reverse (3) directions.

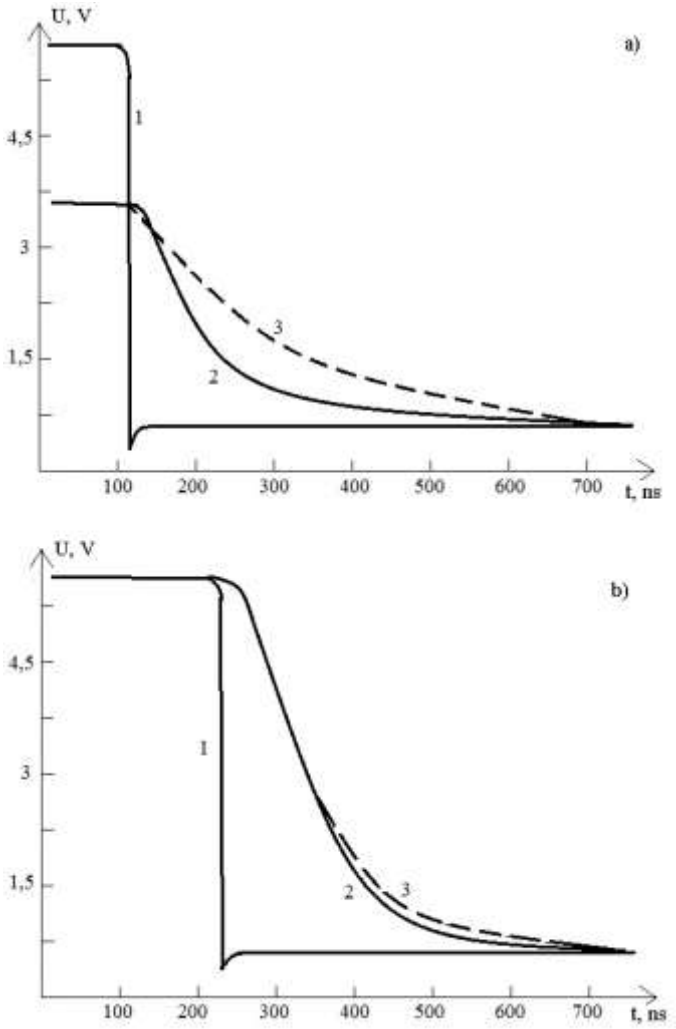

Fig. 3. Switching characteristics for MIS field transistor key (a) and for CMDS (b) key (1 - input voltage; 2, 3 - output voltage before and after impulse exposure, respectively).

The pulses impacting the test circuits had amplitude of 5 V. Experiments have shown that the pulsed substrate current generated in the CMDS inverter is mainly conded by collision ionization, since the drain area potential is very high (V_d = 5V), and the rise and fall times are relatively small (40 ns). This current pulse is localized in the channel drain area of the n-channel MIS field transistor connected to the output inverter node. For switching valves, it is noted that the process of collision ionization proceeds both in the source area and in the drain area and channel of the n-channel and p-channel MIS field transistor. In the first case, the stock area is more susceptible to degradation (when transferring a logical unit) than the source one. In a CMDS gate, the symmetrically proceeding charge transfer process essentially self-limits the accumulation of charge induced by hot carriers, consequently such a gate is characterized by a lower switching time degradation rate than the gate on n-channel MIS field transistors.

For n-channel MIS and CMDS valves, they also removed the drain I – V characteristics at a gate voltage of 5 V (Fig. 2a, b, respectively) before the pulse effect (curves 1) and after it in the forward (curves 2) and reverse (curves 3) directions. Fig. 3 shows the switching characteristics (curves 1 - input voltage; curves 2, 3 - output voltage before and after a pulse, respectively). For p-channel transistors of a CMDS inverter and a CMDS gate, the degradation was insignificant. The asymmetric nature of the curves after a pulse is applied to an n-channel MIS field effect transistor (Fig. 2a) conded by the asymmetric capture of the injected charge, which leads to a local increase in the barrier height in the damaged region of the channel. With forward bias, the drain voltage is applied to this area and can lower the barrier, resulting in a decrease (measured between peaks), the drain current at high voltages on the drain is negligible. With a reverse bias, there is no such effect, since the drain voltage is applied to the unaffected channel area, as a result, the drain current becomes much lower than before the impact. These curves correspond to the substrate current impulse generated by the circuits, consequently, the drain area is either the only one exposed (CMDS inverter) or is exposed to

a greater degree than the source area (n-channel switching valve). A distinctive feature of a CMDS valve is the symmetric nature of the accumulated charge in both the drain and source areas, so the degradation rate in such circuits is the smallest, although the current generated in the substrate is greater than for an n-channel MIS Field transistor. Shown in Fig. 2 results indicate that the configuration of the scheme affects the degradation mechanism.

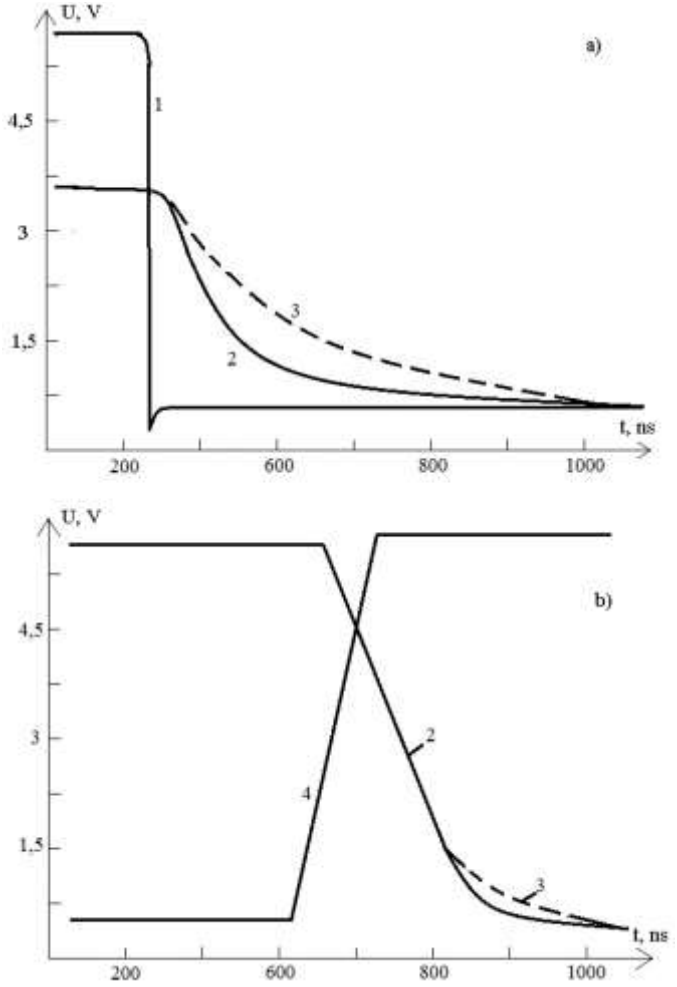

Fig. 4. Characteristics of switching the output voltage for CMDS (a) and n-MIS key (b) (1 is the input voltage; 2, 3 is the output voltage before and after exposure, respectively; 4 is the gate voltage).

The CMDS inverter and n-channel switching valve were also subjected to a destabilizing effect to study the effect of localized charge on switching characteristics (Fig. 4 a, b). In this case, as it can be seen from Fig. 3, the degradation of the CMDS inverter switching time was much lower than that of an n-channel gate. This can be explained by the fact that defects caused by hot carriers in the CMDS inverter n-channel transistor are always localized in an area protected by a depleted field and therefore subject to the effect of reducing the barrier height associated with the drain area. This area is connected to the input node, and switching occurs when the n-channel transistor reduces the potential at that node. For an n-channel MIS transistor, the degraded region is located at the output node and has a large effect on reducing the switching time. The increase in switching time after pulse action for both circuits is insignificant. For the inverter CMDS, this is conded by the switching characteristics are determined by the p-channel transistor, and for the n-channel gate – by the damaged area localization.

III. Conclusion

The results obtained indicate that for VLSI, containing mainly inverter and valve circuits, the degradation of the switching period from one logical value to another in the transmitting valves will be a decisive effect in the general characteristic of the circuits' switching period.

The degradation model caused by hot electrons, which is based on the substrate and drain currents ratio, provides good results for controlling this effect in a wide range of channel length values, oxide thickness, and displacement regimes.

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