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Research and Design of Multi-Channel Telemetry Signal Digital Baseband Transmitter and Receiver Module

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Abstract. In order to realize a system of multi-channel telemetry signal transmitter and receiver module, a design for generating encryption and decryption processing signals in the transmitting module and the receiving module is proposed on the baseband signal processing hardware platform. For the generation of the single-bit telemetry control signal, the idea of using dual-port RAM sequential logic and combinational logic circuits is adopted in the FPGA module, and sorting processing is performed in the DSP module. Combined with embedded system and software radio design, the software design based on C programming language and QUTUS II system simulation are given. The design has passed the hardware and software joint debugging, and can pull up the single-bit telemetry control signal corresponding to the position of the data stream in the case of up to 300 key contents for encryption and decryption processing.

Introduction

The main task of radio telemetry is to realize the transmission of long-distance radio signals, thereby completing tasks such as spatial measurement, information transmission and storage by means of remote detection. Spacecraft, aircraft and near-ground space drones are typical radio telemetry applications. With the continuous development of radio information communication technology, telemetry technology and means at home and abroad have also made great progress. In order to realize the information transmission between the aerial near-ground aircraft and the ground, this topic is based on the standardized software and hardware platform design, using programmable devices and intelligent hardware systems to realize the construction of a new radio multi-channel telemetry system and software radio platform upgrade [1]. This has become one of the important ways to achieve high-speed wireless data transmission in the field of contemporary telemetry technology.

In order to realize efficient and reliable information transmission of the radio multi-channel telemetry system, the quality of the communication channel and information security have received great attention. Therefore, telemetry information transmission and reception needs to follow a certain communication protocol, and at the same time, in order to ensure information security, it is necessary to have certain encryption and decryption processing capabilities. The PCM modulation method is widely used in remote telemetry communication systems because of its high precision and strong anti-interference ability [2]. Therefore, the design adopts PCM modulation mode and adopts time division multiple access modulation mode to realize telemetry and remote control of multi-channel signals. On the basis of ensuring reliable transmission of telemetry data, the security of data transmission is considered, that is, the encryption and decryption of telemetry information [3]. Therefore, it is necessary to generate a specified encryption and decryption key in the master PC, that is, to encrypt or decrypt the specified data stream. To this end, this paper combines the processing of data transmission and encryption and decryption, proposes a multi-channel telemetry signal transceiver module based on FPGA/DSP and related control signal generation scheme, and realizes multi-channel telemetry baseband digital signal transmission and reception through hardware joint adjustment.

Telemetry Signal Transceiver Module Design

Overall Design

The transceiver module includes the transmitter module and the receiver module, and follows the relevant baseband digital signal processing communication protocol.

Transmitter Module Design. The multi-channel telemetry baseband signal transmitting module completes the uplink telemetry baseband signal processing task. In order to realize remote transmission of telemetry information to the flight target, according to the information transmission needs, the data transmission rate is between 1 Mbps and 64 Mbps, and the system clock is 112 MHz. The data encryption control signal is generated in the FPGA and sent to the RF transmitter, as shown in Figure 1.

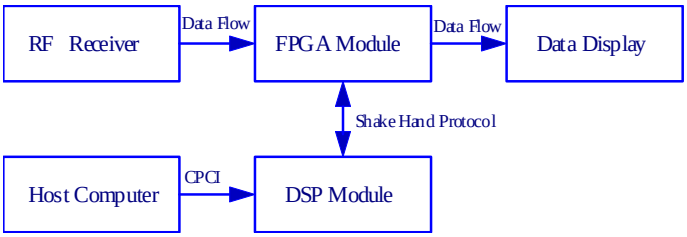

Figure 1. Send module control signal output diagram

In Figure 1, the telemetry data is output from the UART interface of the host PC to the FPGA. In addition, the master PC transmits the telemetry control data to the DSP through the PCI interface and then to the FPGA. It is required that in the FPGA chip, the single-bit control signal at the specified data stream is pulled up according to the key content issued by the DSP to complete the telemetry data encryption operation.

The DSP chip releases the telemetry control data mainly including:

(1) Data transmission frame and DSP controller enable: used to determine whether the DSP and FPGA work;

(2) Key length: The length of the telemetry key can be set in the DSP controller, the maximum length is 300;

(3) Key content: The key used to encrypt the telemetry data usually adopts 32-bit double word, wherein the first 16 bits are sub-frame labels, and the last 16 bits are channel numbers.

Receiver Module Design. The multi-channel telemetry baseband signal receiving module completes the downlink telemetry baseband signal processing task. In order to accept the specified aircraft telemetry signal, the demodulated data stream (telemetry data) is obtained by down-converting the RF analog signal obtained from the RF receiver, and after passing through the high-speed ADC, enters the baseband signal processing circuit for decryption. According to the information receiving needs, its data transmission rate is 1Mbps~64Mbps, and its system clock is 112MHz.

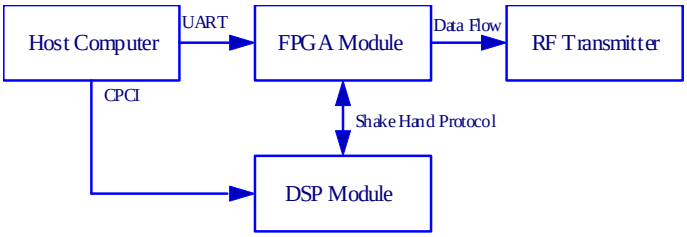

Figure 2. Receive module control signal output diagram

In Figure 2, the DSP chip receives telemetry control data from the host PC through the PCI interface. The processing process of the FPGA chip is: the demodulated data stream obtained from the RF receiver is combined with the key content issued by the DSP, and the single-bit control signal at the specified data stream is pulled up to complete the telemetry data decryption operation.

Frame Structure Design of Multi-channel Telemetry Baseband Signal

The time-division system telemetry signal used in this design divides the data frame according to the time slot, so that different data information is sequenced in time sequence, and the same channel is used for data transmission [4]. Under this requirement, the constructed data stream structure features include the following aspects.

(1) Frame: Since the system adopts time-division multiplexed telemetry, it is necessary to collect at least one telemetry data to form a cyclic data format.

(2) Full frame: All multi-channel telemetry data is cyclically transmitted one week by route, and may include one or more frames.

(3) Subframe: A subframe is formed from the start of synchronization of a certain subframe to the start of synchronization of the next subframe.

(4) Vice-frame: The path of the frame is further divided into a plurality of road signals, and these re-segmentation paths are called one sub-frame in one cycle.

(5) Channel: In the channel parameters issued by the master PC, single bit 1 represents the channel length of 8, and single bit 0 represents the channel length of 16.

(6) Frame header: In the optimal frame synchronization code group, a frame synchronization code group of 16-bit data is taken, and the frame synchronization code group is placed at the end of the frame of one subframe.

(7) PCM data stream: A non-return to zero level code (NRZ-L) is used, where "1" is represented by one level and "0" is represented by another level.

Teletext Transfer Protocol Design

Based on the frame structure design of multi-channel telemetry signals, the telegram transmission packet protocol format of multi-channel telemetry signals is given. The data packet protocol structure required by the baseband signal transmission module is shown in Figure 2.3, including data stream, channel signal and vice. Frame label. On the basis of the protocol structure, combined with the telemetry control data transmitted from the DSP, the single-bit control signal at the specified data stream position is pulled up. The single-bit control signal is at a high level, that is, the encryption and decryption operation of the partial data stream is performed. According to the text transmission protocol, the baseband signal receiving module must also follow the packet protocol structure shown in Figure 3.

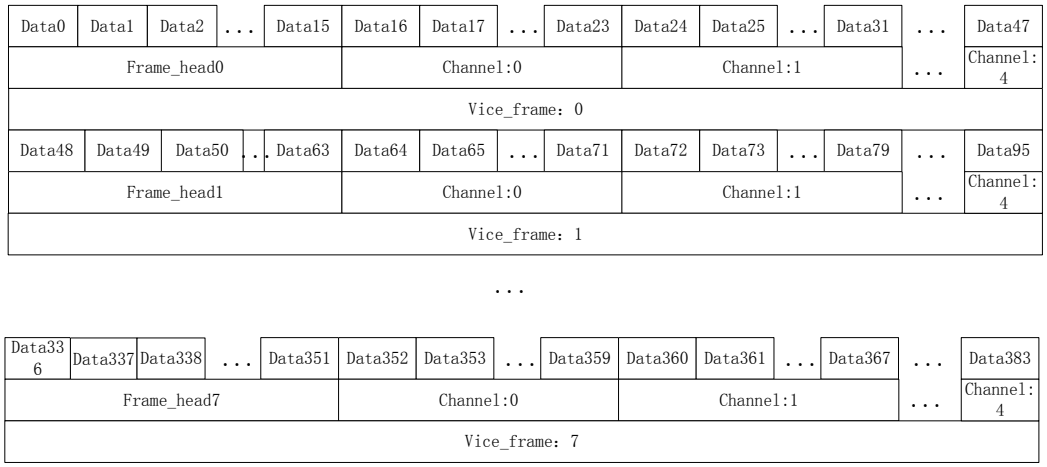

Figure 3. Transceiver module input and output data packet protocol

Baseband Signal Processing Hardware Selection

In order to realize the transceiving and processing of multi-channel telemetry signals, in addition to designing RF transmitters and RF receivers, FPGA and DSP modules are mainly used for multi-baseband signal processing, and UART and PCI are respectively controlled by the master PC.

The interface completes the framing, unpacking and encryption and decryption processing of the data packet to realize the transmission and reception of the multi-channel telemetry baseband signal.

FPGA Chip

Altera not only has the popular Cyclone, Cyclone II series, but also high-performance high-end series such as Stratix, Stratix II, Stratix III and so on. Altera's 65nm Process Stratix III FPGAs feature a rich memory and serial interface that is typically used in complex or high-end applications. The ep3sl340f1517i3n chip represents a high-performance Stratix III family of chips with outstanding advantages [5]: 8:1:1 user I/O / ground / power ratio, this new package pin form not only reduces noise but also user I / O Best in number; optimal tube chip and package level signal loop, which can further reduce signal return path inductance and reduce crosstalk between I/O; adjustable slew rate control allows designers to adjust the edge rate of the signal. For better signal integrity while achieving optimal system performance; dynamic OCT, using the device's OCT resistors reduces component count on the PCB, saves board space and component cost; package decoupling and die capacitance, which reduces Source-drain current surge of gate switching; LVDS buffer enhancement can meet the requirements of high-speed signals for long traces and short traces, and reduce signal attenuation.

DSP Chip

TMS320VC33 (referred to as VC33) is the third generation processor of TI company and TMS320 series introduced in 2001. It supports 32-bit floating-point operation, has 32-bit high-performance CPU, and has 34K *32 bits of storage space [6]. One full-duplex serial Mouth. As a high-performance chip of TI, VC33 has the following advantages: low power consumption, 32-bit high-performance CPU, 34K*32-bit on-chip RAM; program bus, address bus and DMA bus are separated, can be read and written in parallel; 8 extended precision Register; a 32-bit barrel shifter; an on-chip DMA controller that can operate in parallel with the CPU, which can operate on memory in memory without affecting the CPU; a full-duplex serial port, Programmable to 32-bit, 24-bit, 16-bit and 8-bit word lengths, fixed and variable rate two modes of operation; two 32-bit hardware timers; built-in 5x phase-locked loop clock circuit, external The low-frequency clock source obtains the high-speed duty cycle on-chip; the program is self-booting, and the program stored in the external 8-bit, 16-bit or 32-bit low-speed ROM is loaded to any position specified in the 32K high-speed RAM inside the DSP. High speed operation.

Based on the selected hardware, the designed hardware system and test platform are constructed from the devices shown in Table 1.

Table 1. System Debugging Hardware Devices

Device	type	Function
Laptop	Lenovo G480, WIN7 system, 32-bit operating system	runs QUARTUS II9.1SP2 compiler
Industrial computer	CompactPCI MIC3042B8001E-T, WIN XP system, provides CPCI card slot	runs CCS3x/4x compiler and system host software
Display	Samsung S24D390HL	Industrial computer software display
Oscilloscope	The Agilent InfiniiVision MSO-X 3054A	generates a 10MHz clock source.

Telemetry Signal Software Design and Debugging

Software Design of Transceiver Control Signal

Based on master host computer, DSP, FPGA hardware platform, the design of the transceiver module for embedded multi-channel telemetry baseband signal is completed by software design. The single-bit control signal is generated in a manner that uses the sequential logic of the dual port RAM in combination with the combinational logic. First, the dual port RAM writes the key data content sent from the DSP, and then reads the first data content. The data content is compared with the sub-frame number and the channel number to determine whether to pull the single-bit control signal

high. Once the single bit control signal is pulled high, a falling edge pulse signal is generated which determines the conversion of the dual port RAM read address. By repeating the above operations, the writing and reading functions of the telemetry baseband digital signal can be completed. It should be noted that when using this scheme, the key content of a certain length must be sorted, otherwise there will be a case where only the partial single-bit control signal of the data stream position is pulled up, thus leading to the wrong single-bit control signal of baseband information transmission.

The Result of Transceiver Control Debugging

In the single-bit control signal generation, three keys are first generated in the master PC. 0x0001000e, 0x00030003, 0x00030004, respectively, sub-frame 1, channel 14; sub-frame 3, channel 3; sub-frame 3, channel 4, hereinafter referred to as (1, 14), (3, 3), (3 , 4). Grab the corresponding signal in SIGNALTAP. As shown in Figures 6 and 7, sk_single is the generated single-bit control signal, subframe_num is the vice-frame label, and bodao_count is the channel signal synchronized with the data stream (sub-frame content portion). Among them, the (1, 14) pull-up single-bit control signal is shown in Figure 4, and the single-bit control signal pulled up by (3, 3), (3, 4) is shown in Figure 5.

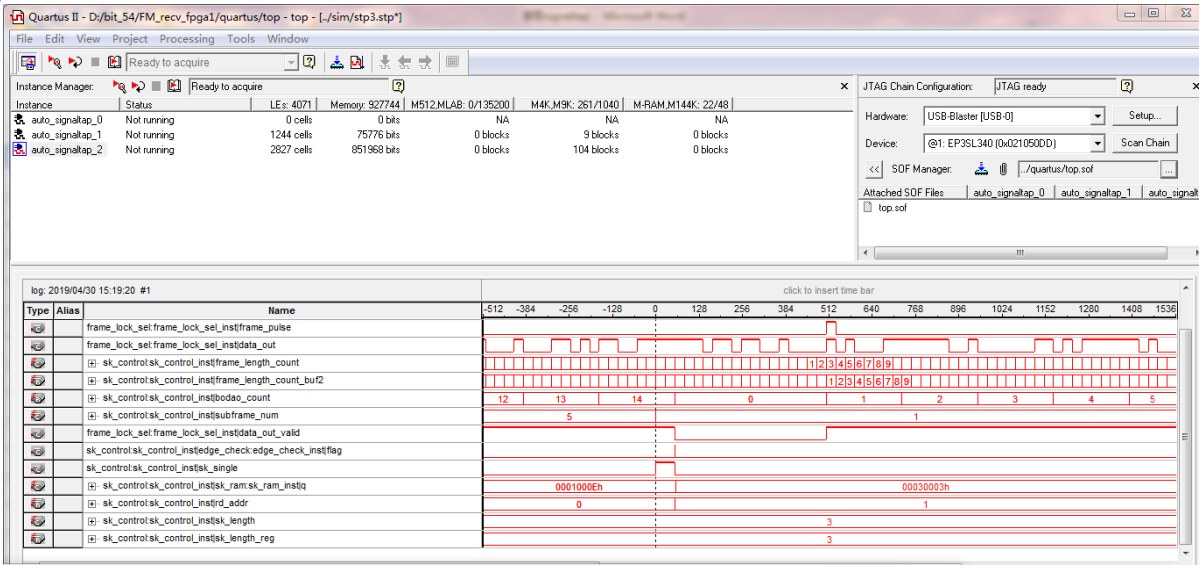

Figure 4. (1,14) single-bit control signal pulled high

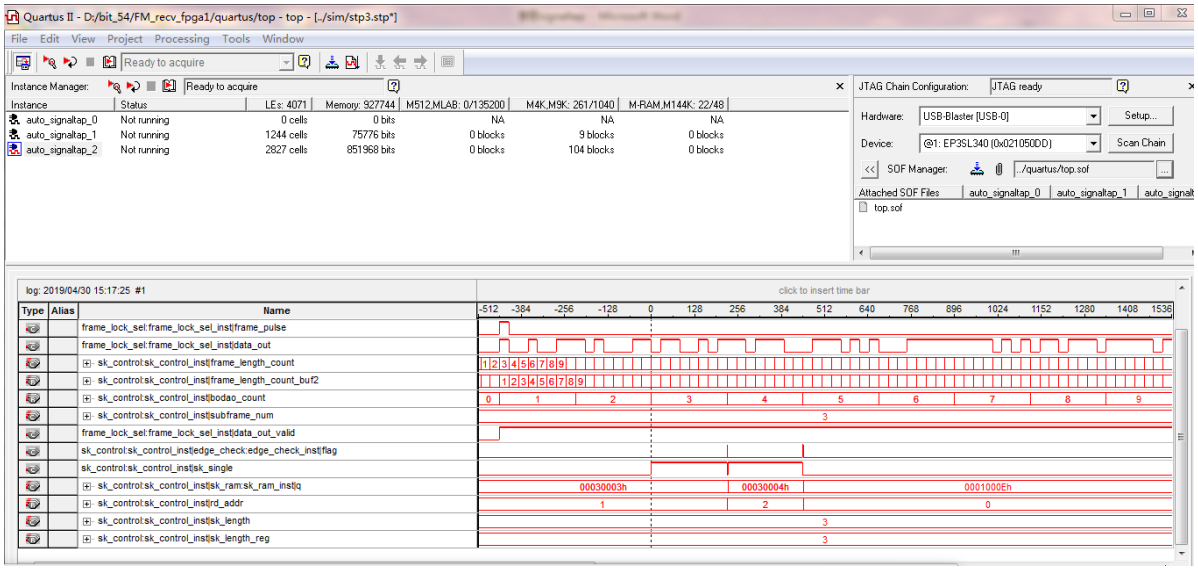

Figure 5. (3,3),(3,4) single-bit control signal pulled high

The experimental test results show that the receiving module can reliably decrypt and obtain the required baseband telemetry digital signal for the encrypted baseband telemetry digital signal sent by

the transmitting module, so that the same channel can be used to complete the reliable transmission of multi-channel telemetry data.

Summary

Aerospace vehicles, high-altitude unmanned aerial vehicles and telemetry satellite communications, due to their special requirements for communication confidentiality and anti-interference, need to be continuously improved in the actual use, and the capacity for encrypting and decrypting the digital information of the telemetry baseband signal is increasing. In this paper, based on the PCM system, the dual-port RAM sequential logic and combined logic output are used to realize multi-channel telemetry baseband digital information simultaneous transmission. The single-bit control signal is pulled up by the control signals given in the protocol, such as the channel number and the vice-frame number, to realize the transmission and reception selection and control of the multi-channel telemetry digital baseband signal. The actual hardware and software system joint debugging has passed the experimental test. Based on the above research and design, the multi-channel telemetry baseband digital signal processing transceiver module can be combined with the corresponding RF front-end to realize long-distance high-rate and high-reliability telemetry information transmission based on software radio technology. The embedded system function based on FPGA and DSP can not only realize the high-speed processing of baseband signals, but also the software radio system can be transplanted. Moreover, based on the current scheme, the intelligent customization and integration of hardware circuits can be further realized.

Acknowledgement

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