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A Method of High Reliability Board Recognition Applied to Dual Redundant Architecture

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***Abstract*—For the electronic equipment of plug-in structure, users can select the sub-boards of different functions for combination applied to different needs, which can increase data processing capacity or reliability of equipment and achieve the goal of meeting the demand quickly and reliably. This is the scheme of the product board. This paper describes a method of high reliability board recognition applied to dual redundant architecture, and analysis all kinds of failure modes. This scheme can ensure the reliable operation and the safety of the equipment under the condition of one-time failure.**

Keywords—dual edundant; high reliability; board recognition

I. INTRODUCTION

Many equipments are board plug-in structure now. A motherboard can be configured with many subboards. Users can select the sub-boards of different functions for combination applied to different needs, which can increase data processing capacity or reliability of equipment and achieve the goal of meeting the demand quickly and reliably. This is the scheme of the product board.

In practice, multiple boards of the same type will be selected to achieve the required function due to the particularity of demand. It is very important to recognize the position of the board among the same boards, because the hardware and software of the board are all the same. The error of position recognition will cause the device to collect the wrong information or send instructions by mistake. Especially for some special areas which require high safety and reliability of equipment puts forward stringent for plate position recognition, such as Aeronautics and Astronautics.

A method of high reliability board recognition applied to dual redundant architecture is proposed in this paper, and the specific method of plate position recognition is described in detail, and analysis all kinds of failure modes. This scheme can ensure the reliable operation and the safety of the equipment under the condition of one-time failure.

II. BOARD RECOGNITION SCHEME

A. Instrument Architecture

The method of board recognition is based on the dual redundant architecture and plug-in structure, which is shown in the following figures.

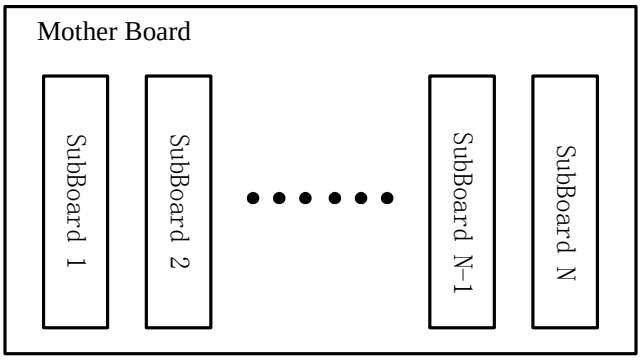

FIGURE I. MOTHERBOARD SLOT POSITION

As shown in the figure, SubBoard 1 to SubBoard N is the slot position of the sub-board. Subboard are divided into control board, communication board, IO input board, IO output board, analog input board, analog output board and other different types of boards according to functions. The subboard communicates with each other through a high-speed serial bus based on nodes, which ensures the fast and real-time communication.

B. Dual Redundancy Scheme of Board Card

The board is dual redundancy architecture to ensure reliability, as shown in the following figure.

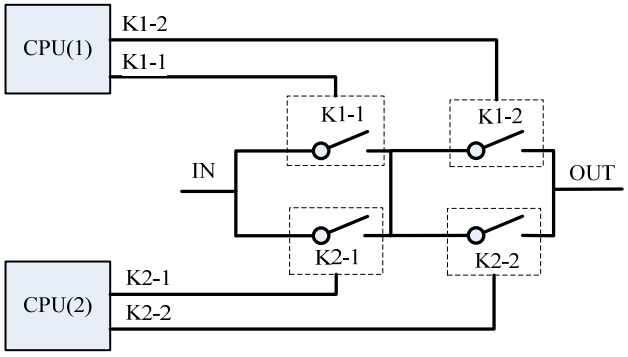

FIGURE II. REDUNDANCY SCHEME

Two CPUs in the board are assigned to different nodes of the bus respectively, and the two CPUs control four executors, which is parallel-series control redundancy scheme. Only if one of the two CPUs sends out execution instructions, the board sends out execution instructions, and this ensures the reliability of the equipment.

C. Circuit Design

The circuit is designed in the mother board to ensure the hardware and software of the subboards are all the same. The circuit is shown in the following figure.

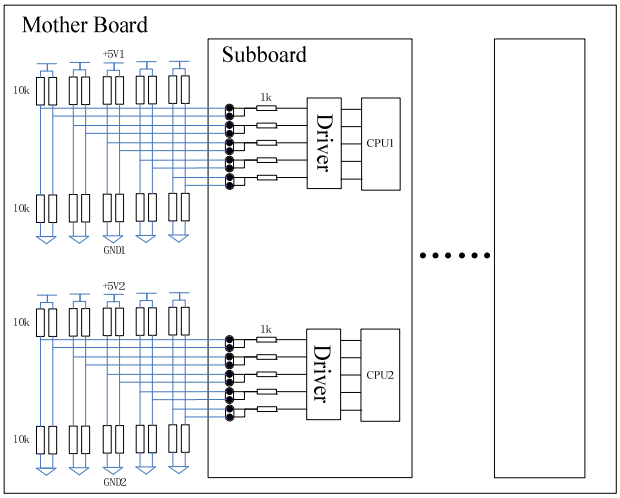

FIGURE III. CIRCUIT OF BOARD RECOGNITION

There are ten point of board recognition on the connector of the subboard for each CPU, which named ID_M[9..0], and every two of them are connected, which means there are five net, which named ID_Z[4..0]. The correspondence is shown in the table below.

TABLE I. THE CORRESPONDENCE OF NET AND POINT

ID_M[9..8]	ID_Z[4]
ID_M[7..6]	ID_Z[3]
ID_M[5..4]	ID_Z[2]
ID_M[3..2]	ID_Z[1]
ID_M[1..0]	ID_Z[0]

Each point is pulled up to VCC or down to GND by resistance. Both pull-up resistance and pull-down resistance are retained on the PCB, and install either the pull-up resistance or pull-down resistance according to the plate position. The resistances are 10k Ω , and in 0603 or 0402 footprint to minimize the volume area.

The net are connected to the driver through a 1k Ω resistance on the subboard, and then to CPU.

D. The Node Distribution

The node distribution are in even check method, which ensures that there are at least two different net between any two nodes. And this can make sure that when there is one net flip due to the circuit fault, the node will not be recognized as the other node leading to erroneous actions.

TABLE II. THE CORRESPONDENCE OF NET AND NODE

ID_Z[4..0]	NODE
00000	1
00011	2
00101	3
00110	4
01001	5
01010	6
01100	7
01111	8
10001	9
10010	10
10100	11
10111	12
11000	13
11011	14
11101	15
11110	16
others	Not defined

III. Failure Mode Analysis

The main feature of this scheme is to ensure the reliability and safety of the system. The instrument can sends out execution instruction under the condition of one-time failure. The following is an analysis of the various failure modes.

A. Resistance on Mother Board Short Circuit or Open Circuit

Take node 1 as example, ID_Z[4..0] are assigned 00000, which means the pull-up resistance are not installed. When there is a resistance short circuit or open circuit, the equipment can work normally. The circuit are shown in the following figures.

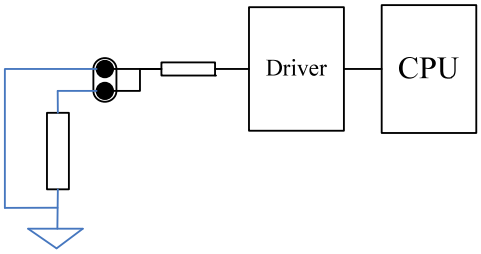

FIGURE IV. RESISTANCE SHORT CIRCUIT

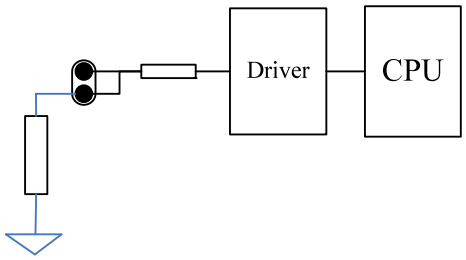

FIGURE V. RESISTANCE OPEN CIRCUIT

B. *Disconnected of Connector*

The disconnect of connector because of the connector not in place or pin problem also do not affect the normal operation of equipment. The circuit is shown in the following figure 6.

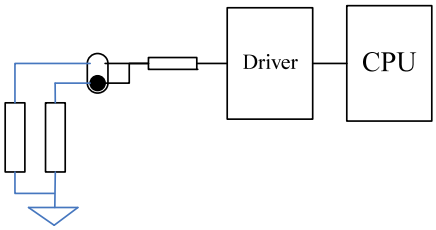

FIGURE VI. CONNECTOR FAILURE

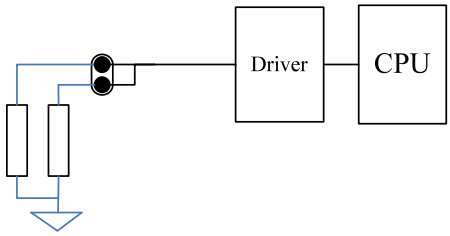

FIGURE VII. RESISTANCE IN SUBBOARD SHORT CIRCUIT

C. *Resistance in Subboard Short Circuit*

Resistance in subboard short circuit does not affect the normal operation of equipment. The circuit is shown in the figure 7.

D. *Resistance in Subboard Open Circuit*

Resistance in subboard open circuit will result in the wrong node number, for example, ID_Z[4..0] are recognized 00001 when the right value is 00000. However, the CPU will not accept and respond to any instruction because the node is not defined. The other CPU will accept the instruction and sends out execution instruction.

E. *Disconnection of Printing Line*

Failure mode is the same as the previous chapter.

F. *Pin Damage of Driver Chip*

Failure mode is the same as the previous chapter.

G. *Pin Damage of CPU*

Failure mode is the same as the previous chapter.

In summary, the method can ensure the reliable operation and the safety of the equipment under the condition of one-time failure.

IV. SUMMARY

The method of board recognition can be applied to high reliability equipment with dual redundancy architecture. The instrument are composed of product boards, users can select the sub-boards of different functions for combination, and this method ensures the hardware and software of the subboards are all the same. At the same time, One-time failure of equipment does not affect normal operation. The method is applied to some project in carrier rocket instruments.

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