A Fast AFC Loop with A Low Power Consumption, Low Phase Noise LC VCO*

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Abstract: This paper presents a fast Automatic Frequency Calibration (AFC) Loop with a low power consumption low phase noise LC voltage controlled oscillator (VCO) at 4.8GHz for WSN Application. The VCO adopts complementary differential negative resistance structure with switch resistor biasing which achieves good phase noise performance and realizing low power consumption. The 6-bits switch resistors array is controlled by auto current calibration (ACC) to get smallest biasing current which can drive the divider-by-two. The 4-bit switch capacitor array provides wide tuning range. We utilize the high frequency prescaler output signal as a discriminating clock and use binary search algorithm to reduce AFC time. The AFC loop circuit is designed in TSMC 0.18μm RF-CMOS process. The post simulated phase noise is −119dBc/Hz@1MHz at frequency of 4.8GHz when the operating current of the VCO core is 0.35mA. The maximum AFC time is 21.8μs with 4-bit AFC. The whole chip size is 0.8×1.2mm2 with testing buffer and pads.

Key words: LC VCO; low power; phase noise; auto current calibration; fast AFC;

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1. Introduction

Wireless sensor network (WSN) consists of distributed sensor nodes in the remote locations and are used to measure the sensor data in remote locations. It is widely used in environmental science, traffic control, disaster prediction, and municipal information infrastructure, etc. The popular application and the environment where WSN is used demand the integration of wireless transceivers in order to achieve lower cost, low power consumption and small size. Frequency synthesizer (FS) is integral in the transceiver circuit to provide local oscillator frequency. The VCO, being the most important part of phase locked loop (PLL) based frequency synthesizer, directly decides the PLL's performance.

For low-phase noise, the VCO is usually designed to have small VCO gain (K_{VCO}) [1]. With small K_{VCO}, however, it is very difficult to cover the required frequency locking range. For this reason, it is common to provide the VCO with digitally controllable frequency tunability. In an LC-tank VCO, switchable capacitor bank is most widely used method [2]. To find the optimum frequency control code of LC-tank, an AFC is needed. However, the overall locking time of FS consists of AFC time and PLL locking time, and the larger number of AFC bit means the longer AFC time. So a fast AFC is inevitable to be designed.

A fast AFC loop with a low phase noise, low power consumption, and wide tuning range LC VCO for WSN is present in this paper. For low power consumption and low cost, the frequency of VCO is 4.8GHz~4.96GHz and a divider-by-two is designed after VCO to get 4 differential quadrature oscillator output at 2.4GHz~2.48GHz. In different environment, the required minimum amplitude of the input signal of divider is varied. In order to achieve the lowest power consumption, ACC is necessary to make the VCO work with the smallest current. To reduce the AFC time, two points of view should be considered. One is to reduce the AFC time by minimizing the number of comparisons and the other is increasing the comparison frequency [3]. In this work, we propose a fast AFC in the second method.

The paper is organized as below: The circuit design including the VCO, the ACC, the divider and the fast AFC are described in section1, the post simulated results are introduced in section 2 and section 3 offers some conclusions.

2. Circuits Structure

Fig.1 shows the simplified block diagram of the whole AFC loop circuit, including a LC VCO, an auto current calibration (ACC), an N-divider and the fast AFC. The 4 bits SW1~SW4 is the output of fast AFC which control the switch capacitor array to provide different tuning curves, and B is the calibration locking signal. The 6 bits B1~B6 control the switch resistor array to provide varied biasing current. V_{top} reflects the amplitude of the VCO output. V_{ref} is reference voltage that decides the amplitude of the VCO output. ACC compares the amplitude of V_{top} and $V_{ref,}$ and then set the 6-bit switch resistor array in order to fix the biasing current and the amplitude of the output voltage of the VCO. V_{tune} is to control the varactor in the VCO. V_P and V_N is differential output of the VCO, and is AC coupled to the input of the N-Divider. The first stage of N-Divider is a divide-by-two divider, which has four quadrature output signals I^+, I^-, Q^+, and Q^-. f_{pre} is the output of prescaler and f_{div} is the output of N-Divider.

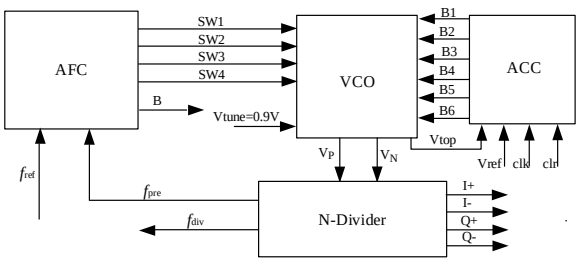

Fig.1 Simplified block diagram of AFC loop circuit

2.1 The VCO Design

The schematic of the LC-VCO is shown in Fig.2. The VCO is based on complementary differential negative resistance structure. The cross-coupled pairs consist of NMOS transistors M1 and M2, and the PMOS transistors M3 and M4. They generate the negative resistance to cancel the loss in the LC tank.

For low-phase noise, the VCO is usually designed to have small VCO gain (K_{VCO}) [1]. For this consideration, the designed K_{vco} is 100MHz/V which is determined by the inductor and the varactor. But it comes with a problem that the output of VCO cannot override the designed frequency differing from 4.8GHz to

4.96GHz. Switch capacitor array is commonly used in wide band VCO [4] [5] [6]. The 4-bit switch capacitor array, as shown in Fig.2, is used in this paper. It will generate 16 frequency tuning curves with low K_{VCO} and better linearity, which can effectively avoid process variation and frequency drifting problems.

Oscillator frequency f can be derived from the following equation:

$$f = 1\Big/\left(2\pi\sqrt{L(C_V/2+C_T)}\right) \tag{1}$$

C_V is the capacitance of the accumulation-mode MOS varactor, and C_T is the total capacitance of the capacitor array.

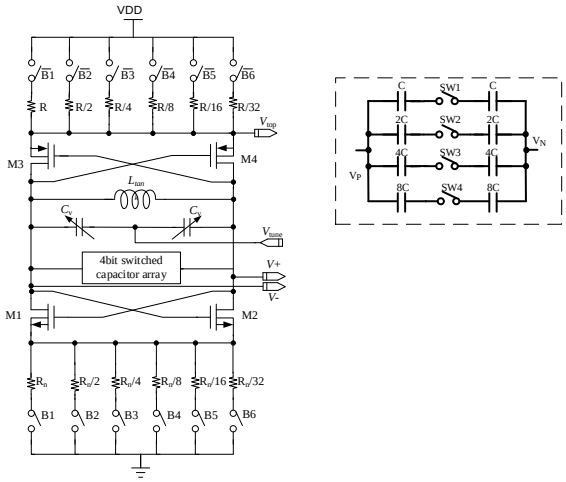

Fig.2 The schematic of the VCO

To reduce current consumption and get a flexible bias current, switch resistor array, instead of the current source, is used in this paper[4] [6]. The bias current is controlled by the 6-bit switch resistor array in the top and the bottom of the VCO in Fig.2. The highest current can be get When the switches is all on, and the lowest current can be get when just switch B1 is on.

2.2 The ACC Design

Cooperating with the resistor array, the ACC searches for the smallest current which can produce enough oscillation amplitude to drive the divide-by-two divider. As shown in Fig.1, a reference voltage V_{ref} must be set to be compared with signal V_{top}, which reflects the amplitude of the VCO output. In every clock

period, the bias current of the VCO will be enlarged till $V_{top} \geq V_{ref}$. Thus, if a proper V_{ref} is set according to divide-by-two frequency divider, the lowest power consumption is realized. This part consists of both analog and digital circuits. In most terrible situation, the calibration time is 63×T (T, clock period). The ACC power is cut off after the calibration is finished.

2.3 The N-Divider Design

Fig.3 shows the simplified block diagram of N-divider. It consists of a 32/33 dual-mode prescaler and a pulse swallow counter. The 32/33 dual-mode prescaler adopts forward phase switching structure. The total divide ratio could be set from 2400 to 2480, covering all required frequencies. f_{pre} is the output of prescaler and f_{div} is the output of N-divider.

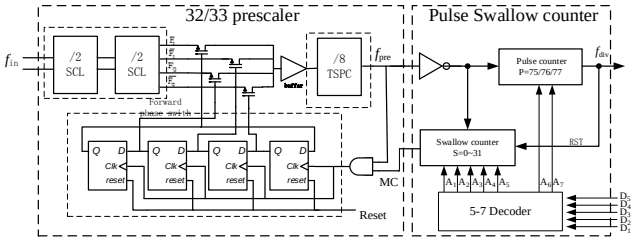

Fig.3 The simplified block diagram of N-Divider

2.4 The Fast AFC

Commonly, the AFC is realized by comparing f_{ref}'s and f_{div}'s counts in a common period T_c. The smaller the counts, the higher the frequency. In general, the T_c is set to 1000T_{ref}.

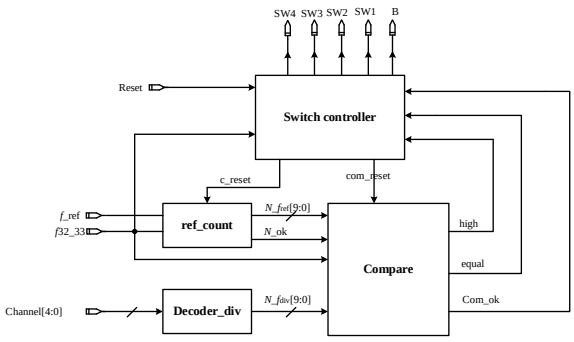

Fig.4 Simplified block diagram of the proposed AFC.

The block diagram of the proposed AFC is shown in Fig.4. The AFC makes the high frequency prescaler output signal f_{pre} as the base clock and compares two values N_f_{ref} and N_f_{div} counted in $10T_{ref}$ and $10T_{div}$ respectively. The switch controller changes 4 bits of capacitor array switchers with binary search algorithm. When the error between two counts is less than 6 which is an acceptable error margin, the four bits switching signals SW1-SW4 are settled. The worst situation needs 4 times of calibration.

3. LAYOUT AND POST SIMULATION RESULTS

Layout of the AFC loop, designed with TSMC 0.18 μm RF CMOS process in Cadence Virtuoso environment, is shown in Fig.5. The whole chip size is 0.8×1.2mm2 with testing buffer and pads.

With 1.8V voltage supply, post simulation is done under the temperature of 27 degrees with Spectre RF tool in Cadence. The current consumption of VCO can be changed from 0.35mA to 3.3mA with the output voltage amplitude of VCO changed from 0.23V to 1.64V. Biasing at 3.5mA, the post simulation of the tuning character of the VCO in TT process corner is shown in Fig.6. The frequency is varied from 4.63GHZ to 5.43GHz, reaching the tuning rang of 20%. K_{VCO} is 100MHz/V when SW4~SW1 is “1011”.

The phase noise performance is shown in Fig.7. When the control bits SW4~SW1 is varied from “0000” to “1111” and the tuning voltage is changed from 0.4V to 1.4V, 16 curves show that the best and worst phase noise is separately −119.4 dBc/Hz and −115.54 dBc/Hz at 1MHz offset from the carrier. Under the control bit “1011”, the phase noise is −118.7 dBc/Hz at 1MHz offset from 4.8GHz.

The post-simulated results of the ACC is shown in Fig.8. When V_{ref}=1.4V, ACC finished working at 0.8 μs. During the calibration, the signal V_{top} is increasing until it equals to $V_{ref.}$ Meanwhile, the amplitude of the VCO output is increasing too. Finally, the amplitude of the VCO output V_{PP} stays at 1.2V. The calibration time is 10×0.08 μs with the clock frequency of 12.5MHz.

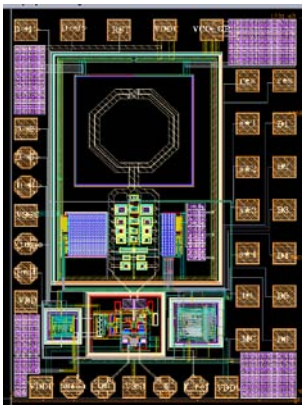

Fig.5 Layout of the AFC loop

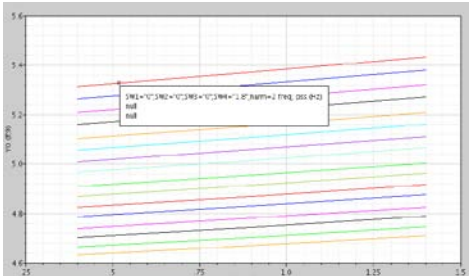

Fig.6 Post simulation of tuning range

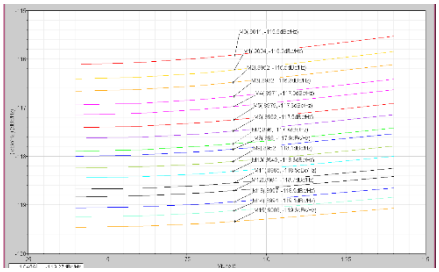

Fig.7 Post simulation of phase noise

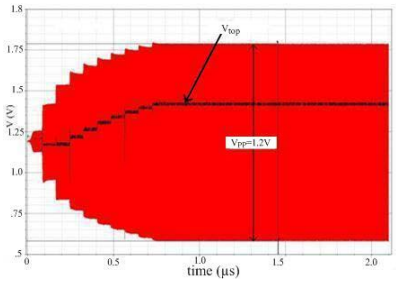

Fig.8 Transient character of the ACC

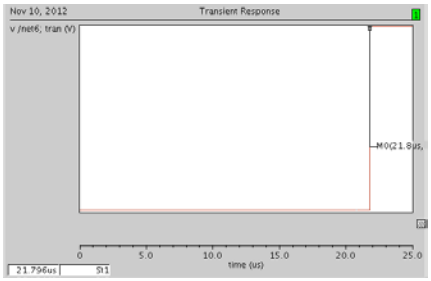

Fig.9 Locking signal “B”

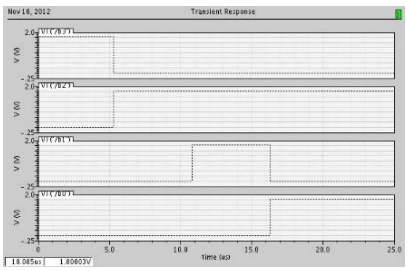

Fig.10 The output of SW4-SW1

The mixed-signal simulation of the whole AFC loop is done with the spectreVerilog tools. Testing in channel 11001, the locking simulation costs 4 times of scheming and the loop locking time is 21.8μs. In Fig.9, the locking signal “B” turns high and Fig.10 shows the output of SW4-SW1 respectively in the locking process.

4. Summary

A fast AFC Loop with a low power consumption low phase noise VCO at 4.8GHz for WSN Application is presented in this paper. With wide tuning range of 20%, the VCO overcomes the frequency drifting perfectly. The K_{vco} of VCO around 4.8GHz is 100MHz/V. Post-simulated results indicate that the phase noise is about −119dBc/Hz at1MHz offset from 4.8GHz. With 1.8V voltage supply, the minimum current consumption of the VCO core is just 0.35mA, realizing the low power consumption. With ACC, the bias current and output voltage amplitude of VCO is varied, make the VCO suitable for various kinds of low power applications. The fast AFC utilizes the output of prescaler as the base clock and calibrates the switch bits of capacitor array with binary search algorithm. In worst situation, the locking time of AFC loop is 21.8μs.

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