A Low Voltage Current-reuse Quadrature Down-conversion Mixer for WSN Application*

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AbstractThis paper introduces a low voltage, low power down-conversion mixerbased on 0.18μm RF CMOS process, the transconductance stage of which uses the current-reuse.The mixer is composed of two identical mixers which share the same transconductance stage,folded switching stage,active load stage,and common-mode feedback (CMFB) circuits. The mixer hassome advantages of low supply voltage, high conversion gain, and low noise figure. The post-simulation results show that, with a power supply voltage of 1V and a input *RF* frequency of 802 MHz,the mixer achieves a conversion gain (*CG*) of 10.7dB, the singleside-band (*SSB*) noise figure *(NF*) is 7.969dB, the input 1dB compression point *(IP_{1dB})* of -15.57dBm, the third-order input intercept point *(IIP3)* is -5.16dBm, and the current consumption is merely 357.1μA.

Key words:low voltage •low power •current-reuse •CMOS mixers •0.18μm CMOS

1 Introduction

Wireless sensor network (WSN), deployed in monitoring area of a large number of low-cost micro sensor nodes, forms a multiple hops self-organizing network system through wireless communication. Its purpose is to be able to real-time monitor, sense and collect nodes interested in deployment of the observer's perception of the object of all kinds of information, and then send out information to the observer through the wireless network. The RF transceiver chip of the project in accordance with the standard IEEE 802.15.4 / ZigBee was designed and implemented using CMOS technology, the schematic of WSN transceiver system

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is shown in Fig.1. With the development of mobile wireless communications device to keep the direction of miniaturization, integration and portability, low voltage, low power consumption, low cost, and performanceis required for WSN applications.

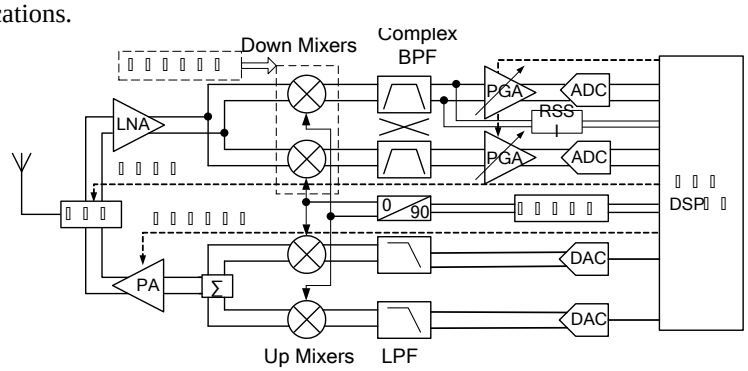


Fig.1 The schematic of WSN transceiversystem

Down-converter mixer, the second stage module of WSN RF receiver system, is to convertRF signal amplified by the low-noise amplifier (LNA) into an intermediate frequency (IF) signal, the entire circuit is completely operating in the RF band. Therefore, the key performanceindicators of down-converter mixer design should include power, linearity, conversion gain and noise figure, and most important, corresponding to the mixer used for WSN, low voltage low power consumption will become a key research direction. This paper proposes a low voltage current-reuse quadrature down-conversion mixer, the current consumption of which is merely 357.1μA from a 1V supply voltage, and yet the conversion gain of which could achieve 10.7dB without deteriorating other performances obviously.

This paper is organized as follows. The first part is the introduction of the paper, the second is focusing on the design of transconductor stage of mixer; the third is the present of proposed mixer. The post-simulated results are reported in the fourth part. Conclusion is in the fifth part.

2 Design of transconductor stage [2]

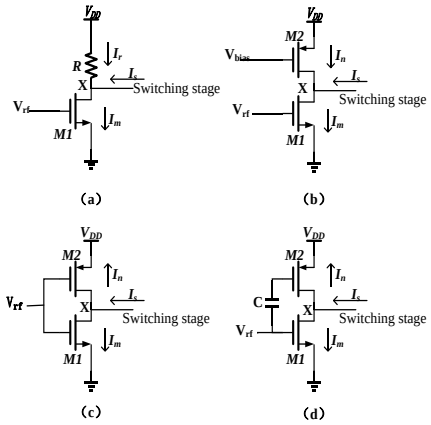


Fig.2 Four different mixer transconductor structure

Fig.2 shows four different transconductor structuressuitable for down-conversionmixer of low supply voltage. The first structure[see Fig.2 (a)] is the simplestone of a load resistor directly superimposed on the transconductance stage, the NMOS transistor generates a radiofrequency current I_m, respectively flow into the switch transistors(I_s) and the load resistor(I_r). The drawback of the first structure is that part of the RF signal will leak to the ground through the load resistor. In order to reduce the I_r, the value of load resistance (R) is necessary to increase, so the operating voltage of the point X will decrease, and then the transconductance transistor ($M1$) will deviate from the saturated region under conditions of low supply voltage. The shortcomings of the first structure can be avoidedusing an active transistor as the load. Therefore, the second structure[see Fig.2 (b)]is obtained by replacing the load resistor (R)with the PMOS transistor. Because of the high output impedance of the PMOS transistor, the RF current I_n flowing through the load is significantly reduced, but still there is a small part of the RF signal leaking to the ground. So considering that, in addition tousing PMOS transistor to increase the impedance value between point Xand V_{DD}, wecan also take advantage of the PMOS transistor to amplify the radio frequency signal. In this way, the mixer can not onlyavoid the RF signal leakage, but also can better amplify the RF signal. Based on the aboveconclusion, a CMOS inverter as the structure of the transconductance stage is obtained[see Fig.2 (c)]. In CMOS inverter, RF signal through the PMOS transistoramplifieris the current reuse principle, which is an effective method to obtain high gain, low noise figure and

low power consumption. The figure shows that the RF currentI_s is equal to the sum of I_n and I_m. Therefore, the total transconductance of such a transconductance stage is equal to the sum of the transconductanceof the two transistors, i.e.g_{mn} + g_{mp}, where$g_{mn}$is the transconductance value of the transistor *M1*, g_{mp} is that of the transistor *M2*. The minimum supply voltage the mixer required is determined by the threshold voltage (V_{th}) and the overdrive voltage(V_{Δ}) of the transistors *M*1 and *M2*.The overdrive voltage of the transistor *M1* and *M2* is calculated as

$$V_{\Delta n} = V_{rfdc} - V_{th} \tag{1}$$

$$V_{\Delta p} = V_{dd} - V_{rfdc} - V_{th} \tag{2}$$

V_{rfdc} is the gate bias voltage of *M1* and *M2*. Therefore, the minimum supply voltage (Vddm), at which the mixer can work properly,can be expressed as

$$V_{dd} = V_{\Delta n} + V_{\Delta p} + 2V_{th} \tag{3}$$

In 0.18-μm CMOS process, the typical value of$V_{th}$is about 500mV, from (3),we can see that the minimum supply voltage (V_{ddm}) is greater than 1V, which cannot meet the supply voltage of 1V. In order to overcome the above drawbacks, the two transistorsin the CMOS inverter should be respectively given DC bias. Fig.2 (d) used the transconductance of the ac-coupled structure. With V_{rfdcn}as the NMOS bias and V_{rfdcp} as the bias of the PMOS transistor,V_{ddm} expression becomes

$$V_{ddm} = V_{\Delta n} + V_{\Delta p} + 2V_{th} + V_{rfdcp} - V_{rfdcn} \tag{4}$$

If the value ofV_{rfdcp} issmaller than that of V_{rfdcn}, V_{ddm} can be reduced, and then the mixer will meet the conditions of a supply voltage of 1V.

3 Design of the proposedmixer

Connecting the current-reuse ac-coupled transconductor with the current switch stage, the mixer structure of this paper to introduce will be obtained.As shown in Fig. 3.

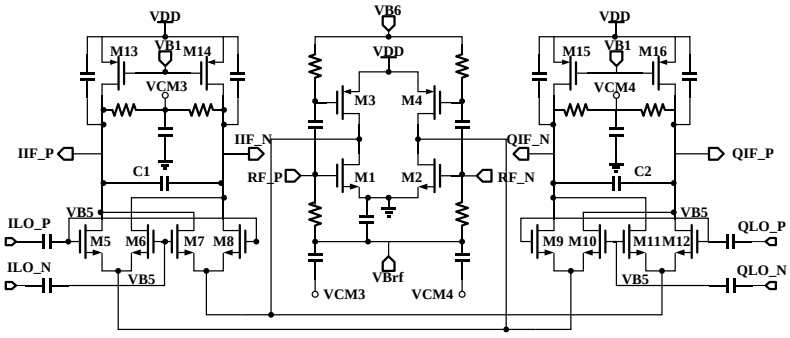


Fig.3 The schematic of current-reuse mixer

In this figure, the transistors M1 to M4 constitute the mixer transconductance stagewith current reuse. By the figure, the transconductance stage is shared by twoway switch ofthe same phase and quadrature, this design is consideringthe same phase and quadrature two lines of symmetry and balance.In addition, in order to get a larger voltage margin and good linearity, the transconductance stage uses a pseudo-differential structure.

Compared with the traditional Gilbert cell, another advantageofthis paper adopts structure is thatuse active transistor instead of load resistance.Fig.3 shows that the transistorsM13toM16 constitute the active load level, at this point,the output in the same pressure drop conditions can get greater load impedance, the voltage margin had no significant effect at the same time,and this is helpful to improve the voltage conversion gain of mixer. At the same time this kind of design can improve the linearity of mixer.

TransistorsM5toM12 constitute the switch pairs, its channel length is designed to be the minimum value, i.e. 0.18μm, so that the switch can achieve the fastest switching speed.

As we all know, there will be two productsin the mixer IF output side, which are the sum-frequency and difference-frequency signalof RF and LO, the difference-frequency signal is the useful component of the IF signal and the sum-frequency signal is an unwanted component, in the circuit output capacitor (C1, C2) role is to filter out the unwanted frequency component.

3.1Design of common-modefeedback (CMFB) circuit

Because the mixer uses a current source load, so in order to stabilize the output common-mode voltage, ensure that the switch on and the driver stage transistors work in the saturation region, the circuit also need an output commonmode feedback circuit (CMFB) [5], Theschematic of CMFB adopted by this design is shown in Fig.4, *VCM3* and *VCM4* connect respectively to correspond to the same

node in Fig.3, the reference voltage V_{ref} is generated by $I_{\mathrm{REF}} \cdot R_{ref}$. So that the load impedance value of the mixer is equal that of the NMOS transistor output impedance and the common mode feedback resistor in parallel. Similarly, in order to avoid the short channel effect and reduce the channel length modulation effect, load transistor channel length is longer.

4 Post-simulation results

Mixer in this article is designed based on a 0.18μm RF CMOS process. The layout of the mixer is shown in Fig.5. The whole of this chip is $1282 \times 976 \mu m^2$.

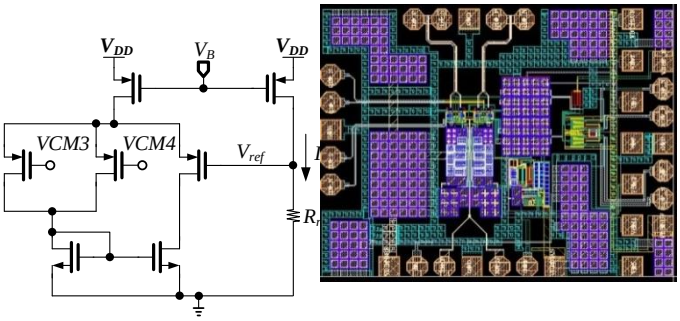
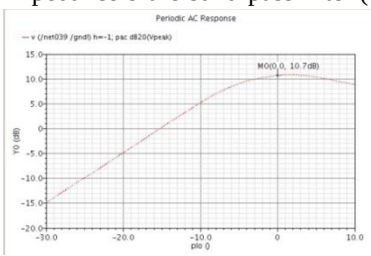


Fig.4 The simplified schematic of the CMFB circuit**Fig.5** The layout of the mixer

All of the following simulation results are obtained in the process angleof TT and temperature of 27degrees,where the input RFis 802MHz, input local oscillator (LO) frequency is 800MHz and LO power is 0 dBm.

The simulation curve of relationship between *CG* with LO poweris shown in Fig.6, the figure shows that, when the LO power is 0dBm, the voltage conversion gain (CG) is 10.7dB, and the corresponding load impedance is the input impedance ofthe band-pass filter (BPF).



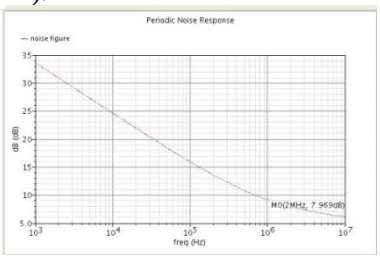


Fig.6 Simulated CG versus LO power **Fig.7** Simulated SSB NF versus IF frequency

The simulation curve of the single sideband (SSB) noise figure (NF) is shown

in Fig.7. The figure shows that the mixer noise figure is 7.97dB @ 2MHz, due to the noise figure is dependent on the mixer input source impedance, and so during simulation the source impedance of the RF port directly usesoutput impedance of the former stage low noise amplifier (LNA).

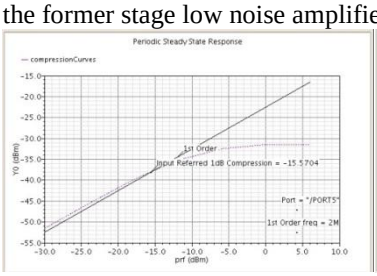


Fig.8 Simulated *IP*1dB

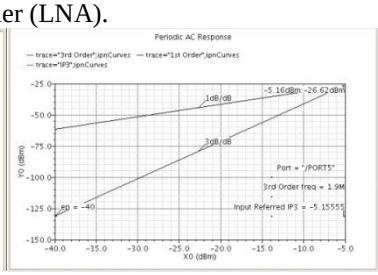


Fig.9 Simulated *IIP3*

The simulation curve of mixer linearity is shown in Fig.8 and Fig.9, which respectivelyare simulation results of the mixer 1dB compression point and third-order intercept point, figure illustrates the mixer IP1dB is -15.57dBm @ 2MHz,IIP3 is -5.16dBm @ 2MHz.

For a better comparison with the advantages of the present structure, the table lists some of the results of other papers and the structure for comparison. As shown in Table 1. The performance of mixer can also be expressed by a quality factor named FOM, figure of merit, the expression of which is as follow[2]:

$$\mathrm{FOM} = 10\log\left(\frac{10^{\mathrm{CG}/20} \bullet 10^{(\mathrm{IIP3}-10)/20}}{10^{\mathrm{NF}/10} \bullet P}\right) \tag{5}$$

Where CG is voltage conversion gain of the mixer in dB, IIP3 is the input third-order point of the mixer in dBm, NF is the noise figure of the mixer in dB, and P is the power consumption of the mixer in W. FOM is proportional to CG and P, while is inversely proportional to NF and IIP3, and then we can summarize that the performance of the mixer is better if FOM is as high as possible.

Table 1 Comparison with other reference

Reference	Freq. (GHz)	V_{DD} (V)	CG (dB)	NF (dB)	IP1dB (dBm)	IIP3 (dBm)	I (mA)	FOM (dB)
1	2.5	0.8	5.7	15.9	-	4.3	3	10.3
2	2.4	1	11.9	13.9	-	-3	3.2	10.5
7	2.4	1	11	14	-	4.1	6.6	10.35
8	0.9	0.9	2	13.5	-	3.5	5.2	7.55
This work	0.8	1	10.7	7.97	-15.57	-5.16	0.36	24.2

Table1 shows that, comparedwith other literature, noise figure and power consumptionperformance of this paper described the down-conversion mixer is significantly improved, other did not significantly improve performance, and linearity instead became worsecompared to other literature.

4 Conclusion

RF module design for the power requirements is getting lower and lower, with the transistor size and supply voltage to decrease, the traditional Gilbert cell can no longer meet the requirements of the application. The proposed current-reuse mixer is a way to solve the low supply voltage low-power design, it greatly reduces the power consumption, while maintaining the other performanceis good.

Simulation results show thatthe design of proposed down-conversion mixer can meet the application requirements of low power supply voltage.

References

1. C. Hermann et al. , "A 0.6 V 1.6 mW transformer based 2.5 GHz down-conversion mixer with 5.4 dB gain and -2.8 dBm IIP3 in 0.13μmCMOS," in Proc. Radio Frequency Integrated Circuit Symp.(RFIC),2004, pp. 35–38.
2. V. Vidojkovic, Johan Van Der Tang, Arjan Leeuwenburgh et al., "A Low-Voltage Folded-Switching Mixer in 0.18μm CMOS [J]" IEEE J. Solid-State Circuits, June 2005, vol. 40, no. 6, PP. 1259-1264.
3. Mahmoudi F. SalamaALAMA C.A.T., "8 GHz, 1 V, high linearity, low power CMOS activemixer", IEEE Radio Frequency Integrated Circuits (RFIC) Digest, 2004, PP. 401-404.
4. T.H. Lee, "5-GHz CMOS Wireless LANs [C]", IEEE Transactions on Microwave Theory and Techniques, vol. 50, no. 1, PP. 268-280, January 2002.
5. B. Razhavi, RF Microelectronics [M], Prentice Hall PTR, 1997, PP. 189.
6. M.Krcmar, "A Broadband Folded Gilbert-Cell CMOS Mixer [J]", IEEE International Conference on Electronics, Circuits and Systems, PP. 820-824, Dec. 2007.
7. E. Klumperink et al. , "A CMOS switched transconductor mixer," IEEE J. Solid-State Circuits , vol. 39, no. 8, pp. 1231 –1240, Aug. 2004.
8. C. Debono et al., "A 900 MHz, 0.9 V low-power CMOS down-con-version mixer, " in Proc. IEEE Custom Integrated Circuit Conf. (CICC) ,2001, pp. 527 –530.