Design of Low Voltage Low Noise Amplifier for 800MHz WSN Applications*

ZhaolongWu, ZhiqunLi +

Institute of RF- & OE-ICs, Southeast University, Nanjing, 210096;

School of Integrated Circuits, Southeast University, Nanjing, 210096;

Key Laboratory of Jiangsu Province Sensor Network Technology, Wuxi, 214135

+**Corresponding author: zhiqunli@seu.edu.cn**

Abstract: This paper presents a 1V low noise amplifier (LNA) for 700~900MHz WSN applications in 0.18μm RF CMOS process.The LNA uses capacitor cross-coupled, current-reused and noise cancellation techniques to reduce noise and power consumption.The simulation results are as follows: The voltage gain is variable with high gain at 22dB and low gain at 0dB. At low gain mode, the input referenced 1dB compression point (IP1dB) is -15dBm and the input 3rd intercept point (IIP3) is 1dBm. The noise figure (NF) at high gain is 2.85dB (@800MHz).It consumes about 0.9mA current from 1V power supply.

Key words:low noise amplifier; low voltage;low power consumption; capacitor cross-coupled; current reuse;

Recently, research of wireless sensor network(WSN) has become more and more popular.WSN nodesare powered by batteries. In order to extend battery life, the power consumption of WSN receivers should be reduced. At the same time, the other performance of the receivers should be remained unchanged. As the first stage of the receivers, the LNAs greatly impact on the performance of the entire receivers. [1-2]

Two types of CMOS LNA topologies have become mainstream circuit implementations: common-source LNAs(CS-LNAs) and common-gate LNAs(CG-LNAs).In recent years, CG-LNAs have gained popularity because the

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input impedance is fully or partially resistive. As a result, the impedance matching can be easily accomplished. Additionally, the impedance matching bandwidth of CG-LNAs is wider than that of CS-LNAs due to the resistive input impedance. Nevertheless, CS-LNAs have the best noise performance. Efforts have been made in the last few years to improve the noise performance of CG-LNAs. Solutions include the transformer-coupled and capacitor cross-coupled. [3-5]

1. Circuits Structure

The schematic of the proposed LNA is shown in Fig.1. Three pairs of MOSFETs adopt capacitorcross-coupled, which increases the effective $G_m$and decrease noise and power consumption. $M_{1,2}$ and $M_{3,4}$are amplifying MOSFETs. The differential signal is inputtedto the source of $M_{1,2}$and the gate of $M_{5,6}$. M_1 and M_5, M_2 and M_6 adopt current-reuse structure to decrease power consumption.

1.1 Capacitor cross-coupled

Effective $G_m$is increasedby adopting capacitorcross-coupledtechnique. The schematic of the boosting effective G_m is shown in Fig.2(a). The structure of the capacitor cross-coupled CG-LNA is shown in Fig.2 (b).

As shown in Fig.2(a), an inverting amplifier is set between the gate and the source of the MOSFET. The inverting amplification value is A. Through the derivation, we can get the expression of the NF [5]:

$$F = 1 + \frac{\overline{i_{\mathrm{nd}}^2}}{\overline{e_{\mathrm{ns}}^2}}\left(\frac{1}{(1+A)g_{\mathrm{m}}R_{\mathrm{s}}}\right)^2 = 1 + \frac{\gamma g_{\mathrm{d0}}}{(1+A)^2 R_{\mathrm{s}} g_{\mathrm{m}}^2} = 1 + \frac{\gamma}{\alpha(1+A)}\Big|_{(1+A)g_{\mathrm{m}}R_{\mathrm{s}}=1} \tag{1}$$

As shown in Fig.2(b), we can deduce[5]:

$$A = \frac{C_{\mathrm{C}}}{C_{\mathrm{C}} + C_{\mathrm{gs}}} = \frac{1}{1 + C_{\mathrm{C}} / C_{\mathrm{gs}}} \approx 1 \tag{2}$$

So the NF of the LNA which adopts capacitor cross-coupled is[5]:

$$F = 1 + \frac{\gamma}{2\alpha} \tag{3}$$

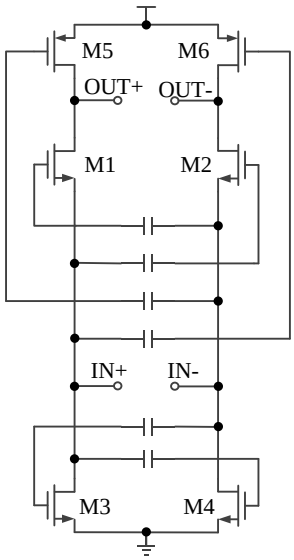
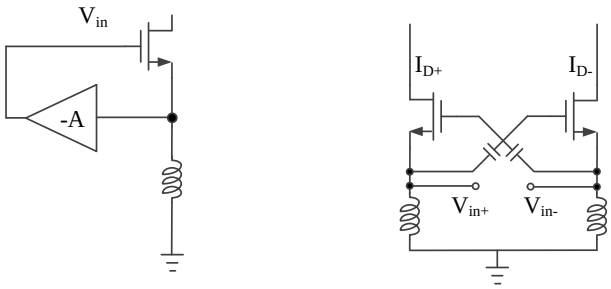


Fig.1Schematic of the proposed LNA

It can be seen that the second part of the equation is decreased by half. Meanwhile, capacitor cross-coupled can reduce power consumption. The reason is given in the next section.



(a)(b)

Fig.2(a)schematic of the boosting effective G_m (b)structure of the capacitor cross-coupled CG-LNA

1.2Impedance matching

Fig.3 shows the small signal representation of the proposed LNA.

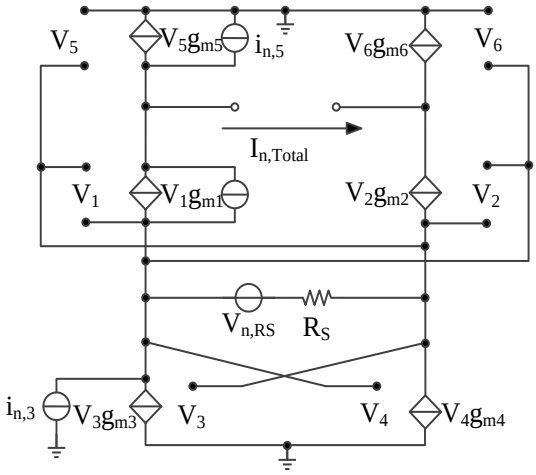


Fig.3small signal representation of the LNA

Ignoring $C_{gs}$of the MOSFETs, the input impedance can be expressed as:

$$Z_{in} = \frac{1}{2g_{m1}} // \frac{-1}{g_{m3}} = \frac{1}{2g_{m1} - g_{m3}} \tag{4}$$

But this formulation only expresses the real part of the input impedance.There exists pathways through the capacitance to the ground. So the imaginary part of the input impedanceis large. By adjusting the capacitance and the W or L of the MOSFETs, we can decrease the imaginary part to accomplish impedance matching.

If the capacitor cross-coupled were not adopted, the input impedance is:

$$Z_{in} = \frac{1}{g_{m1}} // \frac{-1}{g_{m3}} = \frac{1}{g_{m1} - g_{m3}} \tag{5}$$

It can be seen that for the same Z_{in}, capacitor cross-coupled decreases g_{m1}.Socurrentconsumption is also reduced. This is the reason that capacitor cross-coupled can reduce the power consumption.

1.3Noise analysis

The main noise of MOSFET is the drain noise. So we only consider the drain noise, neglecting the other noise.

When the source is matched, the total transconductance is[4] :

$$G = \frac{1}{2}(g_{m1} + g_{m5}/2) \tag{6}$$

So the output noise current due to the source resistor is[4]:

$$i_{\mathrm{n,Rs}} = \frac{1}{2} v_{\mathrm{n,RS}} (g_{\mathrm{m1}} + g_{\mathrm{m5}}/2) \tag{7}$$

The noise contribution due to the $M_{1,2}$comes from two mechanisms that add to the output.

The first mechanism is due to part of i_{n1} entering into $M_{1,2}$ and producing an output current equal to[4]:

$$i_{\mathrm{n1,d}} = i_{\mathrm{n1}} \left(\frac{g_{\mathrm{m1}}}{2(2g_{\mathrm{m1}} - g_{\mathrm{m3}})} - \frac{1}{2} \right) = i_{\mathrm{n1}} \left(\frac{g_{\mathrm{m1}} R_{\mathrm{s}}}{4} - \frac{1}{2} \right) \tag{8}$$

The second one is due to part of i_{n1} flowing throughR_s and producing a voltage V_{43} that is converted into a differential output current. We can get a voltage V_{43} by using a Thevenin equivalent circuit[4]:

$$V_{43} = \frac{i_{\mathrm{n,1}}}{2(2g_{\mathrm{m1}} - g_{\mathrm{m2}})} = \frac{i_{\mathrm{n,1}} R_{\mathrm{s}}}{4} \tag{9}$$

So the total noise current due to $M_{1,2}$ is:

$$i_{\mathrm{n1,d}} = i_{\mathrm{n1}} \left(\frac{g_{\mathrm{m1}} R_{\mathrm{s}}}{4} - \frac{1}{2} \right) + i_{\mathrm{n1}} \frac{g_{\mathrm{m5}} R_{\mathrm{S}}}{8} = \frac{i_{\mathrm{n1}}}{2} \left(\frac{R_{\mathrm{S}}}{2} \left(g_{\mathrm{m1}} + \frac{g_{\mathrm{m5}}}{2} \right) - 1 \right) \tag{10}$$

When the equation (11) is satisfied, the noise of the input $M_{1,2}$ can be cancelled.[4]

$$g_{\mathrm{m5}} = 2 \left(\frac{2 - g_{\mathrm{m1}} R_S}{R_S} \right) \tag{11}$$

The differential noise current from $M_{3,4}$ is[4]:

$$i_{\mathrm{n3,d}} = i_{\mathrm{n3}} \frac{g_{\mathrm{m1}} R_{\mathrm{S}}}{4} + i_{\mathrm{n3}} \frac{g_{\mathrm{m5}} R_{\mathrm{S}}}{8} = i_{\mathrm{n3}} \frac{R_{\mathrm{S}}}{4} \left(g_{\mathrm{m1}} + \frac{g_{\mathrm{m5}}}{2} \right) \tag{12}$$

The noise current from $M_{5,6}$ is[4]:

$$i_{\mathrm{n5,d}} = i_{\mathrm{n,5}} / 2 \tag{13}$$

So the total NF of the LNA is[4]:

$$F_{\mathrm{LNA}} = 1 + \frac{\gamma g_{\mathrm{m1}} (R_{\mathrm{S}} G - 1)^2}{2 R_{\mathrm{S}} G^2} + \gamma (g_{\mathrm{m1}} R_{\mathrm{S}} - 1) + \frac{\gamma g_{\mathrm{m5}}}{2 R_{\mathrm{S}} G^2} \tag{14}$$

Where γ is the MOSFET thermal noise coefficient. When (11) is applied, the NF of the LNA becomes[4]:

$$F_{LNA} = 1 + \gamma(g_{m1}R_S - 1) + \gamma(2 - g_{m1}R_S) = 1 + \gamma \quad (15)$$

2. The simulation results

This paper presents a low voltage low noise amplifier for 700~900MHz WSN applications in 0.18μm RF CMOS process.It consumes about 900μA current from 1V power supply.The layout of the LNA is shown inFig. 4. All the post-simulation is done with a buffer. The post-simulation result of NF is shown in Fig.5. The NF equals to 3.0dB at 800MHz. The post-simulation of S11 is shown in Fig.6. During700~900MHz, S11 is -12.82~-12.7dB; Fig.7 shows the post-simulation of S21. During700~900MHz, S21 is 11.88~14dB; The post-simulation of S22 is shown in Fig.8. During 700~900MHz, S22 is -16.52~16.59dB. At low gain mode, IP_{1dB} is -15dBm(as shown in Fig.9), and the IIP3 is1dBm(as shown in Fig.10).The load of the LNA is down-conversion mixer. We set the input impedance of down-conversion mixer as 2K ohm. The voltage gain is 22dB.The post-simulation results are concluded in TableI.

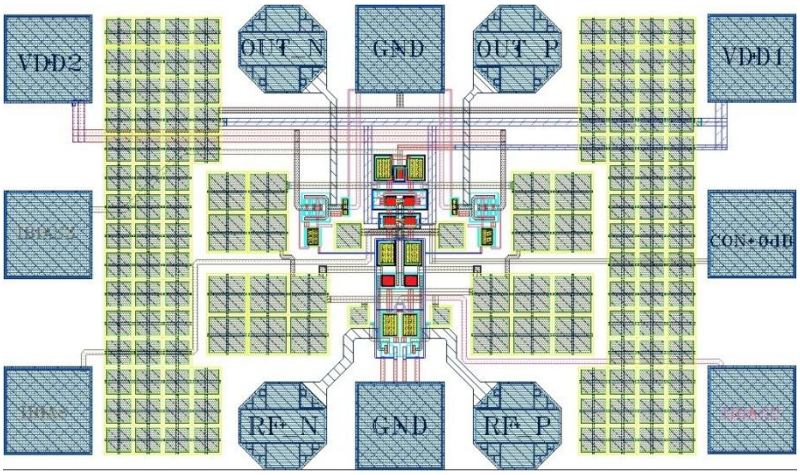
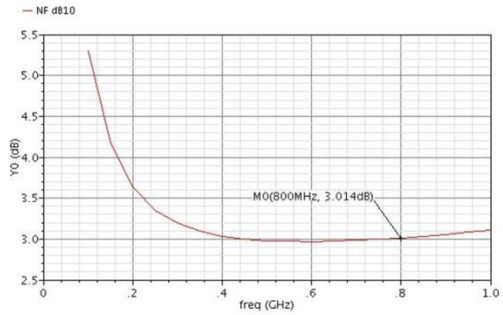


Fig. 4 Layout of the LNA



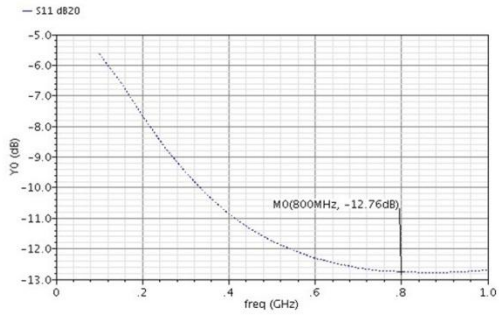
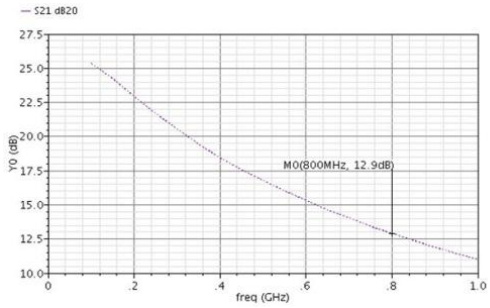


Fig.5Post-simulation result of NFFig.6Post-simulation result of S11



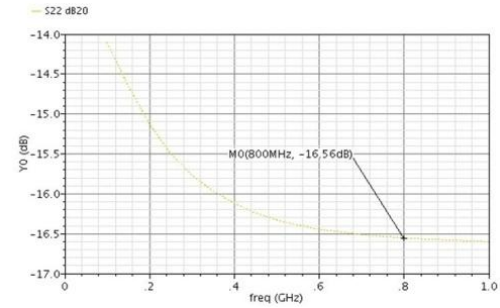
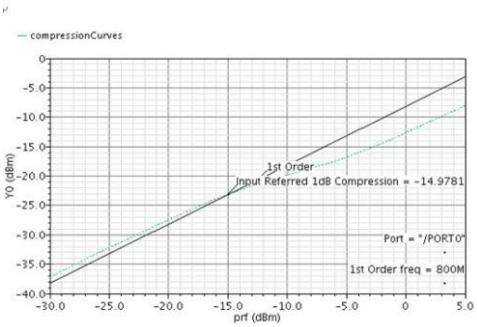


Fig.7Post-simulation result of S21Fig.8Post-simulation of S22



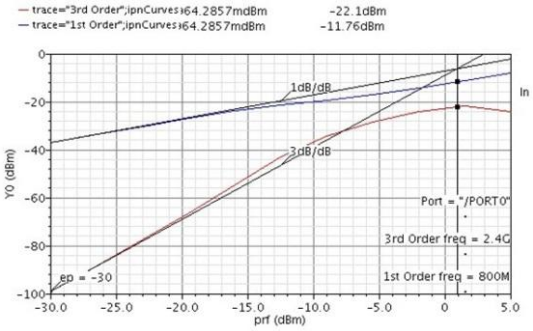


Fig.9Post-simulation of IP_{1dB}Fig.10Post-simulation result of IIP3

Table I.Summary of the LNA post-simulation results

Parameter	value
Supply voltage (V)	1
Power consumption (mW)	0.9
S11 (dB)	-12.82~-12.7
S21 (dB)	11.88~14
S12 (dB)	-55.12~-53.64
NF at high gain mode (dB)	2.82
IP_{1dB} at low gain mode (dBm)	-15
IIP3 at low gain mode (dBm)	1

3. Summary

This paper presents a low noise amplifier for 700~900MHz WSN applications in 0.18μm RF CMOS process. The power supply is 1V. The LNA adopts capacity cross-coupled, current-reuse and noise cancellation to decrease the NF and power consumption. Post-simulation results show that LNA can be fully adapted to WSN system applications.

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