Design of 500MHz Wideband RF Front-end

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Abstract: This paper presents a design of 500MHz wideband RF front-end for P-band radar based on 0.18 μm RF process. The front-end works at the center frequency of 500MHz with 200MHz bandwidth, which transforms single-end signal to differential signal, amplifies it and mixes it with local oscillator signal, outputting an IF signal of 10±5MHz. It adopts noise-canceling to lower the noise figure. It adopts a common-gate input mode to achieve good input match. The post-simulation results indicate that under a 3.3 V power supply, the S11 is less than -20dB in the work frequency band, the conversion voltage gain is 13.5dB. A NF of 8.6 dB and input 1dB compression point of -8.5dBm are achieved with a total current consumption of 11mA.

Key words: RF front-end; noise canceling; high linearity

1. Introduction

Wideband radio receivers have recently drawn significant research interests. Co-operability with other communication devices (e.g., cellular, WLAN) operating in the same spectrum is mandatory, setting especially stringent demands on the wideband linearity of such a receiver. A single-ended RF input avoids the use of an external broadband balun and its accompanying losses. RF front-end module is shown in Fig. 1. The RF signal is mixed at the mixer with the local oscillation signal to obtain the desired intermediate frequency signal (10±5MHz).
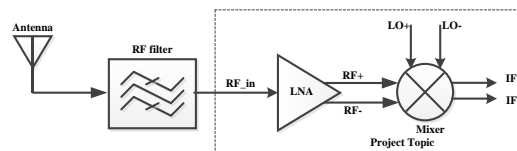

Fig.1 Block diagram of RF front end

Placed at the front end of the entire receiver, the noise of front end has huge impacts on the receiving circuit. Thus it must have certain gain while not introduce too many noises. We should also consider the linearity requirements as the signal is amplified (usually less than 30 dB). We may see significant compression at the output of the mixer. The front end should achieve low noise factor, high linearity, low power consumption and adequate voltage gain.

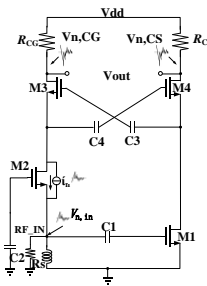## 2．Circuits Design

2.1 Proposed balun LNA topology

Fig.2 Topology of the proposed LNA

Fig. 2 shows a balun-LNA consisting of a parallel operating common gate (CG) and common source (CS) stage. The CG stage realizes wideband input matching and in-phase gain, while the CS stage realizes an anti-phase output signal. In a CG stage only, the noise of the CG transistor would be dominant when the input impedance is matched to R_S ($R_S=1/g_{m,CG}$). However, using a properly designed CS stage this noise (i_n in Fig. 2) can be canceled. The noise current (i_n) generates a noise voltage ($v_{n,in}$) on the source resistor and a larger voltage in anti-phase across R_{CG} ($v_{n,CG}$). The input noise voltage is amplified by the CS stage to $v_{n,CS}$, which is in-phase and fully correlated with $v_{n,CG}$. For equal CG and CS stage gain, the noise due to the CG transistor is fully canceled at the differential output, while the signal contributions to the output signal add up to create a balanced output[1]. The parallel CS-CG topology (or balun-LNA) cancels the noise of the CG transistor in order to obtain a noise figure (NF) close to or lower than 3dB.

The CG stage is biased using an external inductor to obtain low-noise operation and save voltage headroom. The inductor can cancel the capacitive part of input

impedance, making the input impedance purely resistive at the frequency of internet. By using the inductor, the input impedance can be perfectly matched to R$_S$ (50Ω) at the frequency of 500MHz and experiences little fluctuation within the whole band, achieving a good input matching.

The cross-coupled capacitor network can be used for compensating the gain and phase mismatch. This network also can lower the noise contribution of the cascode transistors M3 and M4 by the g_m-boosting effect. In simulation, the cross-coupled capacitors can lower the noise figure by 0.5-0.9dB [2].

To totally cancel the noise generated by M2, the transistors and resistors should satisfy the following formula [3]:

$$g_{m,M2} \times R_{CG}^2 = g_{m,M2} \times R_s^2 \times g_{m,M1}^2 \times R_{CS}^2. \tag{1}$$

To achieve input matching and balanced output at the drain of the cascode transistors, the devices in the topology should also meets this formula:

$$g_{m,CG} \times R_{CG} = g_{m,CS} \times R_{CS} = \frac{A_V}{2} \qquad R_s = \frac{1}{g_{m,CG}} . \tag{2}$$

R$_S$ is usually equal to 50Ω, making the conductance of M2 20ms. Choose the sizes and bias voltage according to the formula above, the noise of CG transistor can be totally cancelled, making no contribution to the total NF. Since the CG noise is cancelled, the CS noise dominates in the LNA. The NF of CS stage can be expressed as

$$F = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{g_m \cdot R_S} \tag{3}$$

To reduce the noise generated by M1 of the CS stage, we choose g$_{m,CS}$ of M1to be 4 times larger than g$_{m,CG}$, then $R_{CG} = 4R_{CS}$[4]. Thus the equilibrium noise voltage at the gate of it can be greatly reduced, and so is the total NF of the topology. By configuring the sizes of the devices of the topology like this, we simultaneous achieve output balancing and noise-canceling at the drains of transistors M3, M4. In simulation, a NF of 2.7-2.8 dB is achieved within the band, proving the excellent performance of the proposed balun LNA.

As derived above, not only the noise of the impedance matching device is canceled, but also its nonlinearity. Assume the nonlinear behavior of M1 can be modeled be the drain-source current which depends nonlinearly on both voltage variations v_{gs} and v_{ds} around their DC bias points. The source signal v_s causes a nonlinear drain-source current i_{ds} which is converted into a nonlinear voltage v_{in} at the input via the (linear) source resistor. The nonlinear input voltage v_{in} can be

written as

$$v_{in} = av_s + v_{NL}, \qquad\qquad (4)$$

where the α represents Taylor coefficient and v_{NL} contains all unwanted nonlinear terms. The output voltage of the CG-stage and CS-stage can be written as

$$v_{out,CG} = ((1-\alpha) \cdot v_s - v_{NL}) \cdot \frac{A_V}{2}, \qquad v_{out,CS} = -(\alpha \cdot v_s + v_{NL}) \cdot \frac{A_V}{2}. \qquad (5)$$

After subtraction only the linear signal remains

$$v_{out,diff} = v_{out,CG} - v_{out,CS} = v_s \cdot A_V. \qquad\qquad (6)$$

In conclusion, all noise and distortion currents generated by the CG-transistor can be canceled, irrespective of whether produced due to nonlinearity of the transconductance or nonlinearity of the output conductance.
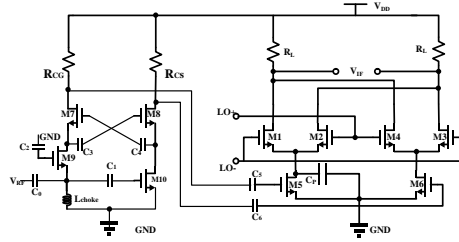
2.2 Design of RF Front-end

Fig.3 Schematic of the front end

In Fig. 3, the principle of RF front-end topology is shown. The output of balun LNA is connected to the Gilbert double balanced mixer by direct coupling. The differential signal is interposed on the gate of transforming transistor of the mixer, mixed with the local oscillator and converted to differential IF signal at the drains of switching transistors M1-M4.

2.2.1 Bandwidth Analysis

There are seven RF signal nodes in the circuit shown In Fig. 3, which are the signal inputting node, the drains of CG and CS transistors, output nodes of balun LNA, the drains of transconductance transistors of the mixer. The real parts of impedances of cascode transistors of balun LNA and the switching transistors of the mixer are very small seen from the source. These nodes don't limit the overall bandwidth. Under the condition of input matching, though accompanied by large amounts of parasitic capacitances, the real part of input impedance is only equal

to 50Ω. The impedances of output nodes of the balun LNA are relatively high than other nodes (R_{CS} 100Ω and R_{CG} 400Ω respectively), making the pole at these two nodes dominant. The choice of the transconductance transistors of the mixer should be careful to avoid introduction of large parasitic capacitances, thus not decreasing the bandwidth significantly. The simulation indicates that, in our design of 500MHz RF front end, the input matching coefficient S11 is less than -20dB from 400MHz to 600MHz and is less than -10dB within a bandwidth of 400MHz around the center frequency; the conversion gain changes only a little within the band and will decrease fiercely only when input signal frequency is down below 300MHz, which proves the good performance of the topology.

2.2.2 Noise Analysis

To simplify the calculation, transistors are assumed to have infinite output impedance and the bias current source of the CG-transistor is assumed to be ideal. Furthermore only the thermal noise of the resistors and of the transistors is taken into account. The noise factor of balun LNA can be expressed as [4]

$$F = 1 + \frac{\gamma \cdot g_{m,CG} \cdot (R_{CG} - R_{CS} \cdot g_{m,CS} \cdot R_S)^2}{R_s \cdot A_V^2} + \frac{\gamma \cdot g_{m,CS} \cdot R_{CS}^2 (1 + g_{m,CG} \cdot R_S)^2}{R_s \cdot A_V^2} + \frac{(R_{CG} + R_{CS}) \cdot (1 + g_{m,CG} \cdot R_S)^2}{R_s \cdot A_V^2}, \tag{7}$$

where the second part is the contribution of the CG transistor, which can be totally cancelled with adequately designed dimensions of the devices of balun LNA, making the third part dominant in the total noise factor. A_V denotes the total voltage gain of the balun LNA, equaling

$$A_V = g_{m,CG} \cdot R_{CG} + g_{m,CS} \cdot R_{CS}. \tag{8}$$

The third part can be expressed as

$$F_{CS} = \frac{4 \cdot \gamma \cdot g_{m,CS} \cdot R_{CS}^2}{R_s \cdot g_{m,CS}^2 \cdot R_{CS}^2} = \frac{4 \cdot \gamma}{R_s \cdot g_{m,CS}} \quad . \tag{9}$$

We can see, by improving the transconductance of CS transistor, the noise factor of the topology can be further optimized.

The noise of the mixer stage is complicated. Every device in the circuit contributes some to the total output noise. Of all the noise sources, the thermal noise and flick noise are the most important [5]. But the flick noise is only prominent at the frequency down below corner frequency f_C, equaling

$$f_C = \frac{K}{4\kappa T}\omega_T , \tag{10}$$

which is approximately from 500 kHz to 5 MHz, where K is a process-related coefficient. So the flick noise is not important in this design (with an IF at 10 MHz). In our analysis of the noise factor of the mixer, this part is ignored, assuming abrupt LO transition with a 50% duty cycle at the same time. The equivalent noise at the input of the mixer can be expressed as [6]

$$\overline{V_{n,in}^2} = 2\pi^2 \left(\frac{C_P^2 \cdot \omega^2}{g_{m,S}^2} + 1\right) \cdot kT \cdot \left(\frac{\gamma}{g_{m,C}} + \frac{\gamma \cdot C_P^2 \cdot \omega^2}{g_{m,S} \cdot g_{m,C}^2} + \frac{2}{g_{m,C}^2}\right), \qquad (11)$$

where the $g_{m,S}$ and $g_{m,c}$ denote the transconductance of switching transistors *and transforming transistors of the mixer respectively, C_P is the parasitic* capacitance at node P, as shown in Fig. 3. We can judge from the formula that the existence of C_P is the reason why the noise of switching transistors would contribute to the output noise. According to the equation (11), we should configure the circuit to minimize the C_P and maximize $g_{m,C}$, thus optimizing the noise characteristic. However, the $g_{m,C}$ experiences a tradeoff with linearity requirements and is limited by the power consumption. As we know

$$IP_3 \propto V_{GS} - V_{TH} \;\;, \;\; \overline{v_{n,in}^2} \propto \frac{4kT\gamma}{g_m} = \frac{4kT\gamma}{2I_D}(V_{GS} - V_{TH}) \;\; . \qquad (12)$$

The dimensions of the transistors and the bias voltage should balance the power consumption, noise performance and linearity. The simulation shows, the noise figure of the mixer is 12-13dB, and the 1-dB compression point is around -3dBm with respect to a R_S of 300Ω, which would not deteriorate the linearity of the front end.

2．The post-simulation results

This paper presents a wideband RF front end for 400~600MHz P-band radar applications in 0.18μm RF CMOS process. It consumes about 11mA current from 3.3V power supply. The layout of the LNA is shown in Fig. 4. The post-simulation result of NF is shown in Fig.5. The NF equals 8.6~8.8dB. The post-simulation of S11 is shown in Fig.6. During 400~600 MHz, S11 is -23~-20 dB; the post-simulation of conversion gain is shown in Fig.7. The conversion gain is about 12.7dB with0.2dB fluctuation when the IF frequency changes between 5MHz and 80MHz; the post-simulation of IP_{1dB} is shown in Fig.7. IIP_{1dB} is -8.5 dBm. The IP_{1dB} is achieved by date fitting on Origin using the date obtained in post-simulation.
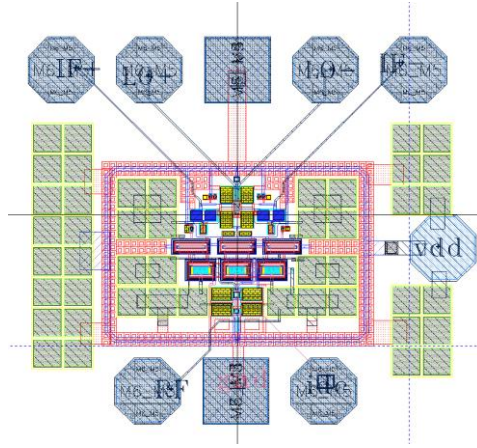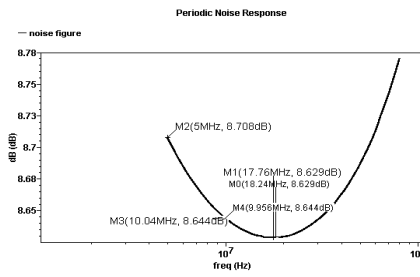
Fig. 4 Layout of the LNA

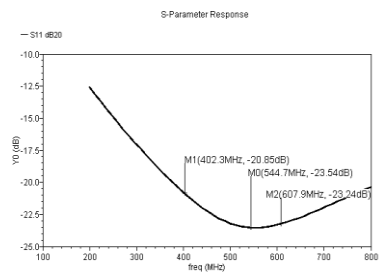**Fig.5** Post-simulation result of NF
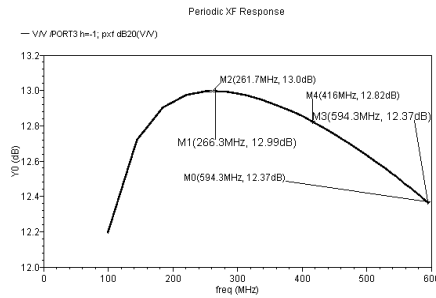

Fig.6 Post-simulation result of S11
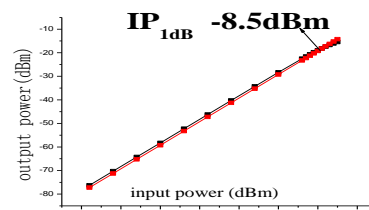

Fig.7 Post-simulation of conversion gain

Fig.8 Post-simulation of IP$_{1dB}$

The overall post-simulation result is shown below:

Parameter	value
Supply voltage (V)	3.3
Power consumption (mW)	36.1
S11 (dB)	-25~-20
Conversion gain (dB)	12.8~13.2
NF (dB)	8.6~8.7
IP_{1dB} (dBm)	-8.5

3. Summary

This paper presents a wideband RF front end for 400~600MHz P-band radar applications in 0.18μm RF CMOS process. The front end adopts linearity enhancement, noise cancellation to decrease the NF and improve the linearity. Post-simulation results show that LNA can be fully adapted to P-band radar system applications.

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