

Systems Model Analysis for Iterative Concurrent Design Processes and Its Application to Design of Precision Mechatronics

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Abstract—We propose a novel methodology of knowledge sharing in mechatronic R&D department by the integration of information repository (IR) using minimal organizational restructure. Through computer simulation and system dynamics, we successfully encompass this concept into a systematic, top-down and inclusive model to assess the advantages and disadvantages of the strategy. The servo-mechanical-prototype configuration in Hard Disk Drives (HDDs) R&D division was analyzed as an illustration of the methodology. Our simple yet comprehensible and replicable model reports encouraging results and improvements: lower process cycle times and their variations, as well as augmented systems capacity and stability.

Keywords- Concurrency; hard disk drives (HDDs); mechatronic R&D; system dynamics

I. INTRODUCTION

In the thin profit margin and short life-cycle mechatronic R&D environment effective process planning in mechatronics systems design projects can enable the execution of rapid design cycles and the delivery of competitive time-to-market while maintain stringent quality specifications and all other relevant cost considerations. To tackle the challenge of multi-disciplinary collaboration of servo engineering, mechanical design, and prototype fabrication, in the authors' recent work [1], a modal parametric identification framework has been proposed as a novel yet practical approach to identify critical feedbacks and crosstalk parameters between the servo engineering and mechanical engineering functions. A new information and workflow structure is then derived in [2] to realize the modal parametric identification concept. The key idea of the new workflow structure is the proposal of a central information repository in which real-time design information can be parsed and retrieved by different functions to enable the execution of concurrent design activities. However, no further quantitative analysis and evaluation of the concept are provided, due to the complexity of analyzing the multi-stage mechatronics design process with concurrent information and work flow.

System Dynamics (SD) models are recognized for being an effective means to convey and facilitate systems thinking and substantiate managerial changes to stakeholders [3] [4] by providing a quick (rough-cut) yet panoramic means of

understanding the system behavior without being pedantic with issues of model input data and prediction of precise numerical levels. In this paper, we propose a novel SD model for the mechatronics design process that incorporates high fidelity Discrete-Event Simulation (DES) concept to describe the flow of individual units in the highly iterative work processes. The integration of useful concepts from DES enables a strong detail-oriented perspective yet retains uncomplicated convenient aspects of a business process modeling tool. The key contribution of our work is the development of a system dynamics (SD) simulation model of the mechatronics design process to study the feasibility, strengths and shortcomings of the proposed central information repository workflow structure. The ultimate aim of the paper is not to build large scale, complicated DES models where the conclusion can be drawn vastly from quantitative yet manipulatable results, but to build a simple yet useful model primarily targeted at managers to understand about the complexities of designing the mechatronics processes with IR.

II. COLLABORATIVE MECHATRONIC R&D

The need for an integrative approach in planning mechatronics design processes has received substantial interest in literature. For instance, [5] proposes a systematic integrated system design method to achieve certain desired separation properties. A centralized R&D research team design and management is presented in [6] to focus on big impact and long-term innovation. The challenges of collaborative business process integration across autonomous subsystems are discussed in [7].

A mechatronics design process generally involves the collaborative work of Servo, Mechanical, and Fabrication teams. The process is initiated by Servo team, who drives mechanical systems specifications in order to achieve the required dynamics performance. Once the design information become available, they are used to drive the Mechanical design work, which comprises various forms of structural analysis and design. Upon completion, mechanical and structural specifications are then communicated to the Prototype team for rapid product prototyping, and laboratory performance testing. Test results and data are then collated and forwarded to the Servo design team for interpretation and analysis. If the test results are not satisfactory, the design cycle is repeated to improve the current design version. This

continues until all test results are satisfactory and all performance specifications are achieved. In view of the importance of competitive time-to-market of new products in mechatronics industries, the current design process flow poses serious inefficiencies due to its strictly sequential and iterative execution nature.

Therefore, it is necessary to understand the behavior of R&D systems in order to establish a set of policies that control the flow and interaction of key information among multidiscipline teams. In the authors' previous contribution [2], a novel concept of an information repository (IR) is proposed to enable information sharing and work concurrency. This is illustrated in Fig. 1, where the information flow is depicted with bi-directional arcs from Mechanical to Prototype and vice versa. In the proposed mechanism, the information obtained from prototype department will be immediately uploaded into the IR and available for retrieval by the Servo and Mechanical teams in real time. Hence, both mechanical and servo team will be able to initiate (part of) its work based on the data pulled from IR.

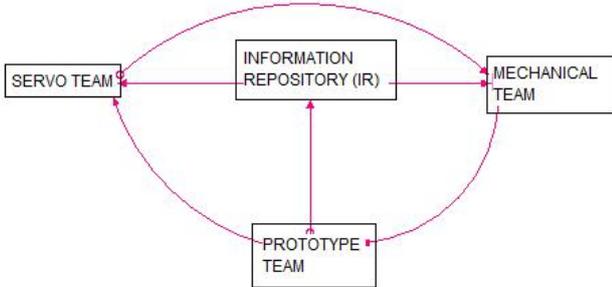


Figure 1. Revised information flow among departments with information repository (IR).

III. SYSTEM DYNAMICS MODELING OF MECHATRONICS DESIGN PROCESS

A. Simulation of Existing R&D Work-Flow Process

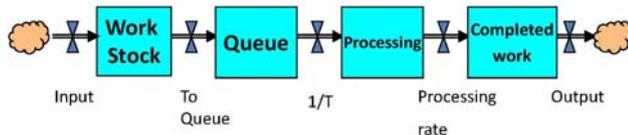


Figure 2. Basic process simulation with stock and flow representation.

Fig. 2 illustrates the model structure of any single stage in the design process. Every product design concept is modeled as a single unit of work that flows through the processes. Unlike in manufacturing systems, these work entities essentially represent information (design specifications, simulation models, etc.) rather than physical material. The design is first stored in Work Stock waiting to join the queue, where Work Stock is modeled as a stock representing the set of unscheduled design work in this stage. Once a design is prioritized based on its importance and urgency, it is pushed in the Queue to wait behind other planned work. Each unit that enters the process remains in

that stage for a period of time (in units of days) equivalent to the average work process time with some random variation modeling the presence of process uncertainties. After the

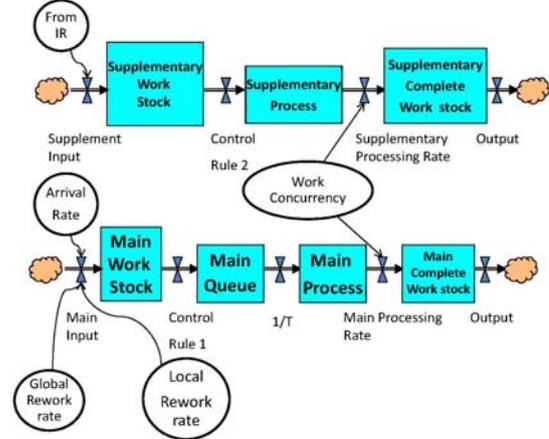


Figure 3. Main work with auxiliary work.

actual design process (Processing) is performed, it is transferred to finished stock (Completed work) waiting for the next stage. In a continuous and sequential process, finished stocks from the preceding stage are also defined as the incoming stock for the following stage. The flow valve in front of each incoming stock is triggered to open only when the preceding design stages have been completed.

B. Integration of IRs

We have identified four sub-design stages that can utilize the information pushed by Prototype teams: S1 Control Design & Simulation, S3 Stability Analysis, M1 Mechanical System Modeling and M2 Finite Element Modeling (FEM) and FE Analysis (FEA). The information triggered by the stage P4 Defining Target Specifications uploads the data into the IR. To model this, each of the four design stages is artificially split into two stages: a main stage which handles the usual flow of work described above; and supplemental stage that takes charges of work initiated by information retrieved from the IR. A model diagram of this is illustrated in Fig. 3. At any time, the team works on at most one of the two stages. The modeling of the supplemental stage follows essentially the same structure as the main stage but, as observed in Fig. 3, there is no queue phase in this sub-model. The rationale for this is that the task is restricted by main stage (Lower flow), i.e. if there is design in queue waiting to be processed, the supplementary stage (Upper flow) cannot be activated. The rule dictates that the team will utilize its resources to solve the most important jobs first, and switch to supporting jobs when there is no job at the uttermost importance.

IV. COMPUTATIONAL STUDY

The computational studies' objectives are to investigate the benefits and implications of the IR implementation in the design process in two aspects: IR influences on overall cycle time and system stability and the effectiveness of the at different design stages. The processing times of all design

tasks are modeled using the Monte Carlo statistical function in iThink. The software generates exponentially distributed random numbers with mean of 5 days for all processing times, except for tasks S3 and M1 that take 15 days to

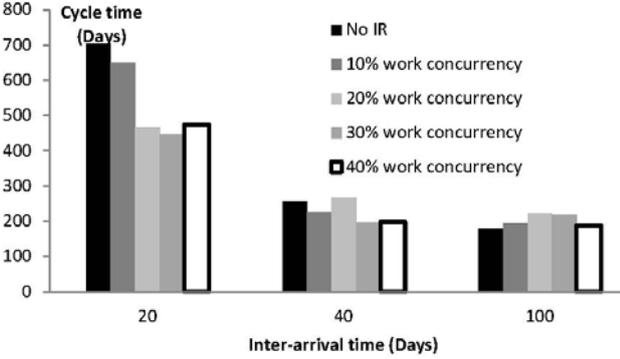


Figure 4. Cycle time result for integration level redesign rate 50% with Inter-arrival time of 30, 70 and 150 days.

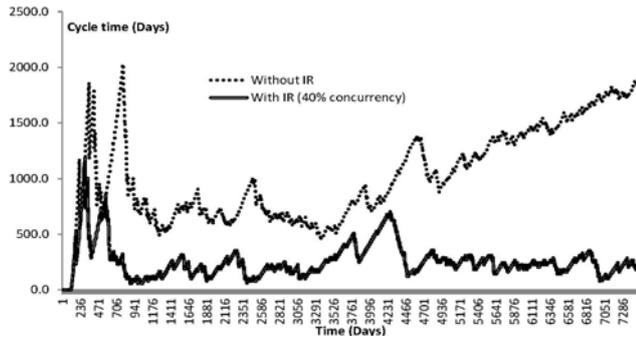


Figure 5. Cycle time result for integration level redesign rate 30% with Inter-arrival time of 20 days.

complete one design. Both of these stages perform complicated design and analysis work and they require longer times to complete.

The department level (i.e. Servo, Mechanical and Prototype) rework rate is set at 5% in the base case, and the integration level (at the end of every iterative cycle) redesign rate is varied from 10% to 90% with 10% intervals. The times between arrivals of product concepts were simulated using an exponential distribution, at various mean time between arrivals. Each simulation is run for significantly long period (at 7500 days) to observe the trend of design cycle times.

A. Cycle Time with IR: Concurrency

Fig. 4 shows the average cycle time performances for selected inter-arrival times at an integration level redesign rates (ILRR) of 50%. In each case, the work concurrency level was varied between 0 (no IR) to 0.4. There are three categories that represent three levels of inter-arrival times of the new product concepts: overload (smallest inter-arrival time), balanced and under-load (largest inter-arrival time). It can be observed that for most cases, the mean values of cycle time when there is no IR are significantly higher than those

of IR implementation cases. In balanced scenarios, which most resemble normal working setting, as we increase work concurrency, the performance improves with lower cycle time.

Fig. 5 presents the results of the cycle time performance when the arrival rate of upstream design work matches the capacity of the design team. It can be observed that without IR implementation, the system exhibits instability, with the cycle time escalating in an unbounded manner. On the other hand, with the IR implementation, the system is stabilized, with lower average cycle time while steady-state was achieved. This again is due to the improvement in the design process capacity with the IR, providing the additional buffer to cope with marginal overloading scenarios.

B. Bottleneck Processes: Iterative Designs

In practice, it might not always be feasible to implement work concurrency at the bottleneck stages. In this section, we randomly assign the process times to shift the bottleneck stage to other stations. In all cases, the stages with the longest processing times (lowest work capacity) are not located in neither S1, S3, M1 nor M2 as previously assumed. Instead, they are all at the prototype department as it practically takes the longest processing time to materialize specifications into archetypes.

TABLE I. CYCLE TIME FOR NON-BOTTLE NECK CASES

Case	Parameter	Work concurrency				
		0%	10%	20%	30%	40%
1	Mean	151.39	162.56	195.28	189.37	168.3
	Variation	85.71	115.05	168.35	133.89	110.00
2	Mean	182.54	199.43	205.58	232.39	188.26
	Variation	108.87	91.50	120.39	143.84	126.68
3	Mean	348.30	499.05	588.40	440.74	418.05
	Variation	294.73	358.05	565.16	312.92	382.56

Table I presents the cycle time results obtained at normal load (near to full capacity) for the three scenarios presented above. The results indicate an increase in cycle time when IR (work concurrency) is implemented. This implies that there is a performance degradation which is contrary to the observed behavior from the previous section. The processing rate of servo and mechanical design stages increases due to the enabling of work concurrency from IR implementation. This however also contributes to the rate of redesign work in the system, which leads to congestion at the bottleneck (prototyping) stage. Table II supports this reasoning, and shows the numbers of designs transferred to the prototype department for realization and amount of redesigns reverted back to servo team. As observed, the numbers of prototypes to be fabricated increase when work concurrency is allowed.

We can summarize the above discussion in the causal loop diagram in Figure 6. An increase in the cycle time leads to a decrease in observed performance. Increases in cycle time can result from an increase in erroneous information being parsed and hence requiring additional re-work. A decrease in observed performance can prompt the management to increase the implementation of work concurrency through the use of IR. On the other hand, increasing the level of concurrency implementation also increases the integration level redesign if IR is implemented

at non-bottleneck stages. This is because concurrency accelerates the flow of process, which in effect increases the arrival rate, cycle times and queue at the bottleneck stages. The deterioration of performance may then spur the manage-

TABLE II. NUMBERS OF DESIGNS FOR REALIZATION AT PROTOTYPE DEPARTMENT AND NUMBERS OF INTEGRATION LEVEL REDESIGNS

Case	Parameter	Work concurrency				
		0%	10%	20%	30%	40%
1	Mean	391	402	407	402	400
	Variation	93	93	97	110	95
2	Mean	181	185	183	184	184
	Variation	30	37	35	35	29
3	Mean	162	183	174	176	167
	Variation	32	47	40	41	35

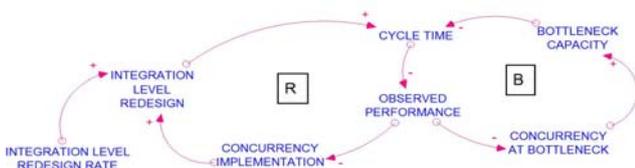


Figure 6. Casual Loop Diagram for error propagation and corruption effect. R: Reinforce loop. B: Balancing loop

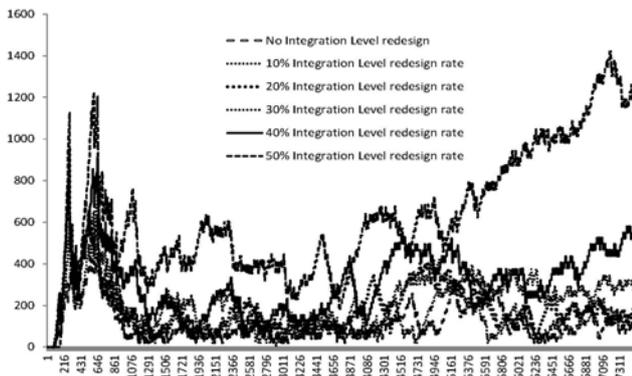


Figure 7. Cycle time result with progressive integration level redesign rate, 23 day inter-arrival time and 20% work concurrency.

-ment to increase the implementation of the work concurrency. Hence, a reinforcing feedback loop is formed that prevents the amplification of cycle time.

We next study the effect of the integration level redesign rate of the system performance, by fixing the work concurrency level and varying the work concurrency enabled. Fig. 7 shows the result for case 1 with Inter-arrival time of 23 days and 20% work concurrency. The same trend is observed in all other cases with different combinations of work concurrency and inter-arrival time. At low integration level redesign rate (at 10% – 30%) the steady state is disrupted marginally. This can be explained by the fact that process capacities at these rates can overcome the rework effect. However, from 40% of redesign rate and above, the increase in loading from the redesign work quickly outstrips the improvement of the process capacity, hence destabilizing the system and the cycle times escalate rapidly due to the congestion.

The primary insight of these results is that even though IR can enable the work concurrency at the individual stages, unless the IR is implemented for bottleneck stages, the overall performance is not necessarily better. This also highlights the critical importance of reducing the integration level redesign rate, since this can lead to capacity improvement substantially without reducing processing time at individual stages.

V. CONCLUSION

In this paper, we propose a novel information sharing mechanism named information repository (IR) to facilitate concurrency and knowledge sharing among teams in commercial R&D division, especially pertaining to servomechanical structure used in the HDD industry. The proposal is cost effective as it does not require organization restructuring and manpower reassignment. The outcomes are encouraging with decreased cycle times, together with reduced variations in the two parameters. Moreover, the IR intervention is demonstrated to be reasonably effective in maintaining system stability in moderately overload scenarios which otherwise cause the process to be unsteady. On the other hand, there are some precautions that must be made before IR implementation. Firstly, the work stations benefited from IR must be the bottlenecks in the process, or else the reengineering efforts are futile. Secondly, extra efforts have to be made in order to ensure the information's absolute accuracy entered into the sharing system. Further works could include dynamic manpower allocations to enhance the utilization and cost-saving of R&D corporations, reengineering methodologies to manage the IR efficacy in non-bottleneck stations and algorithms to optimize inter-arrival times.

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